

Fig. 1
NODE
INTERCONNECT

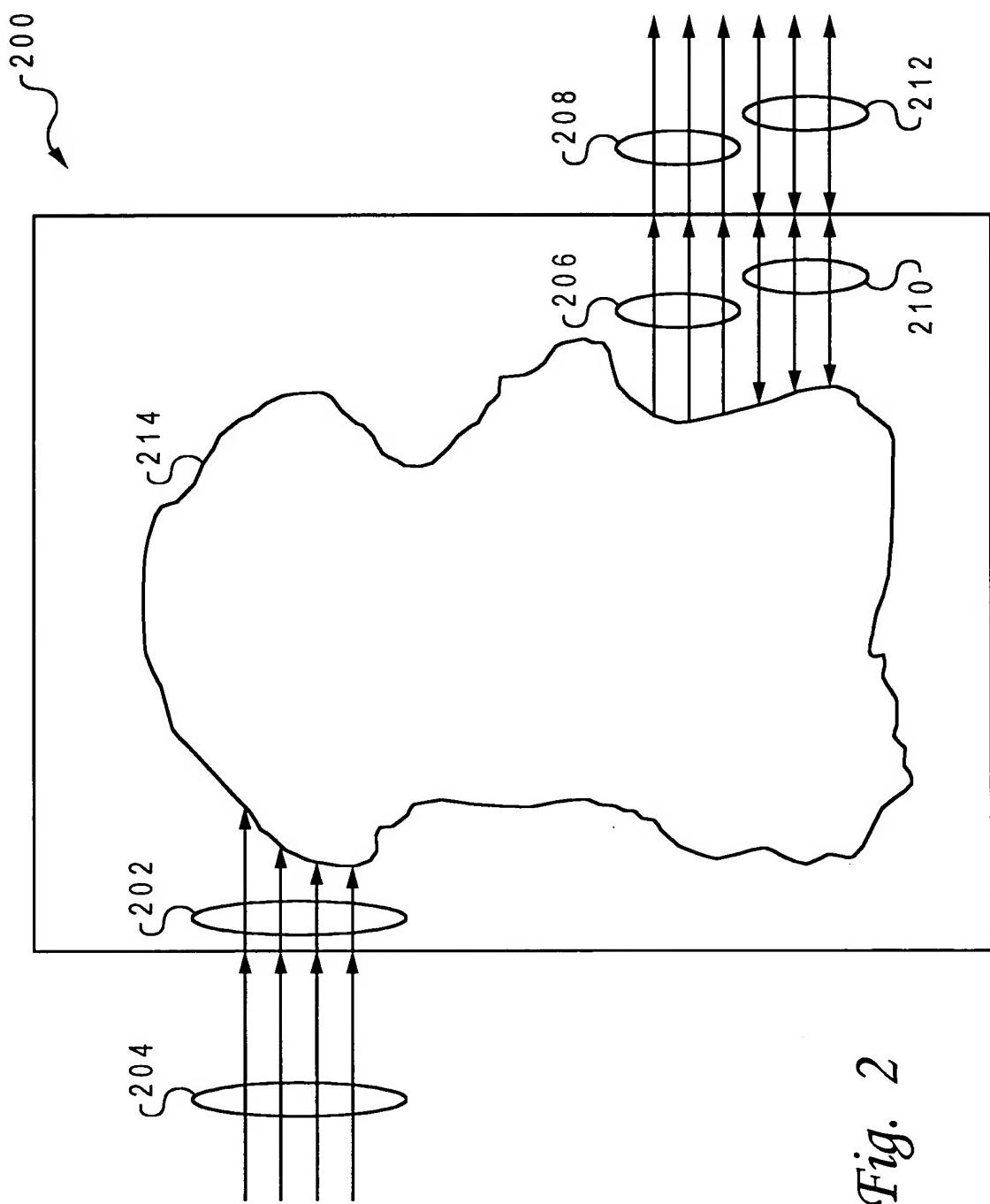


Fig. 2

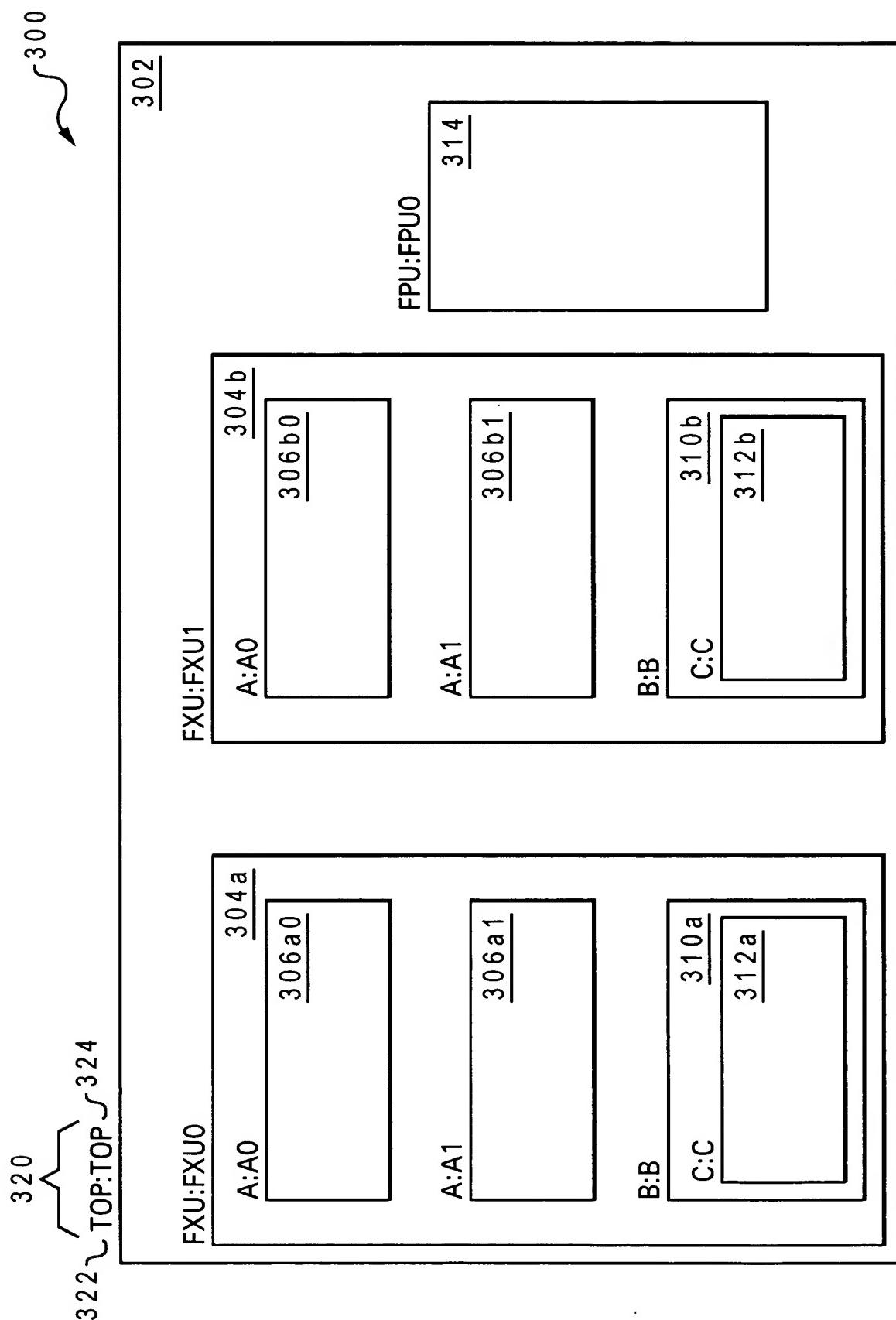


Fig. 3

400

```
ENTITY A IS
  PORT
  (
    ...
    );
END A

ARCHITECTURE A OF A IS
...
BEGIN
  ...
  --## statementA
  --## statementB
  --## statementC
  ...
  --## statementD
  --## statementE
  --## statementF
  ...
END;
```

402 -- port_list

404 -- signal declarations

406 -- HDL code describing design

408 -- HDL code describing design

410

Fig. 4A

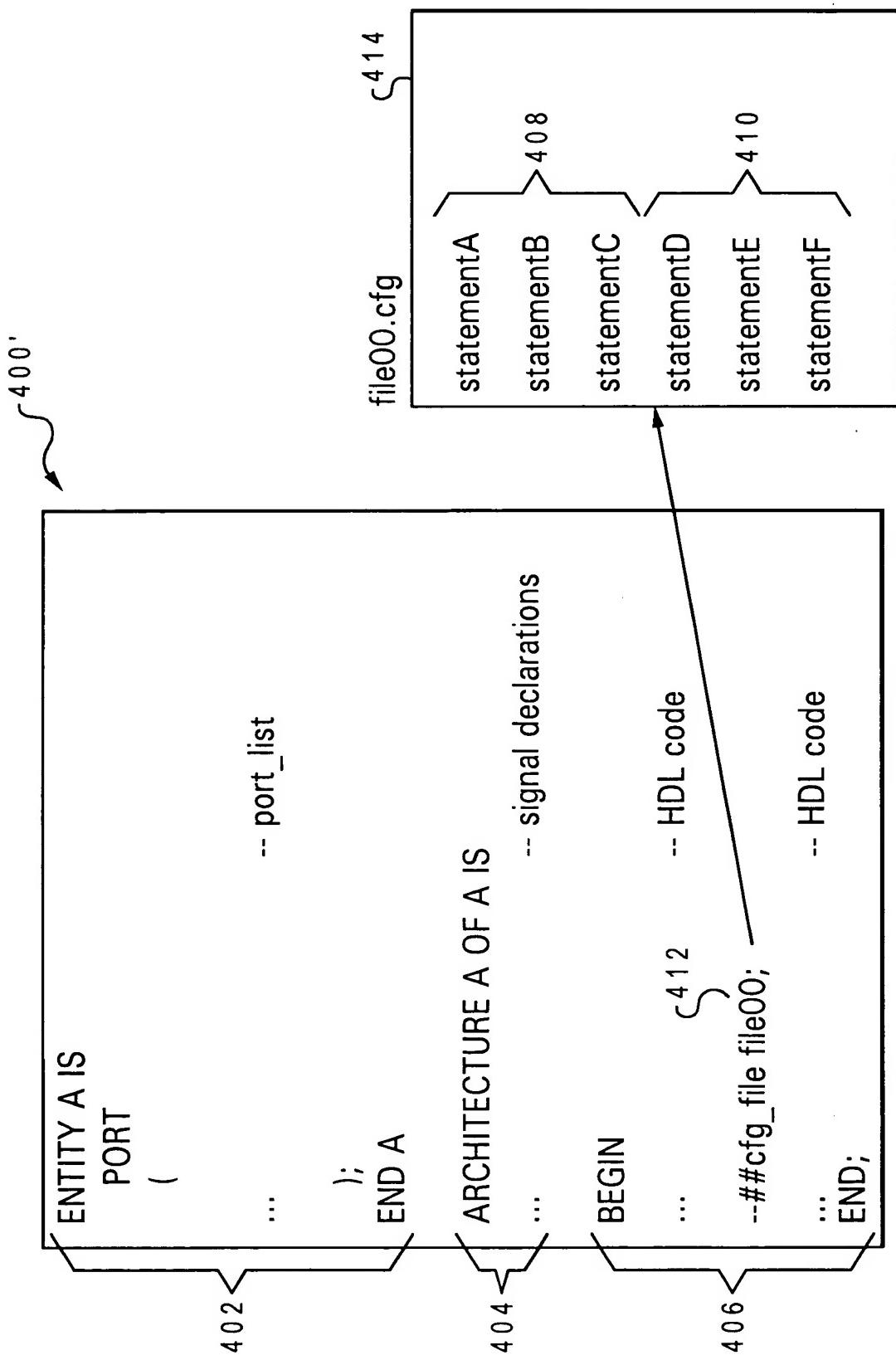


Fig. 4B

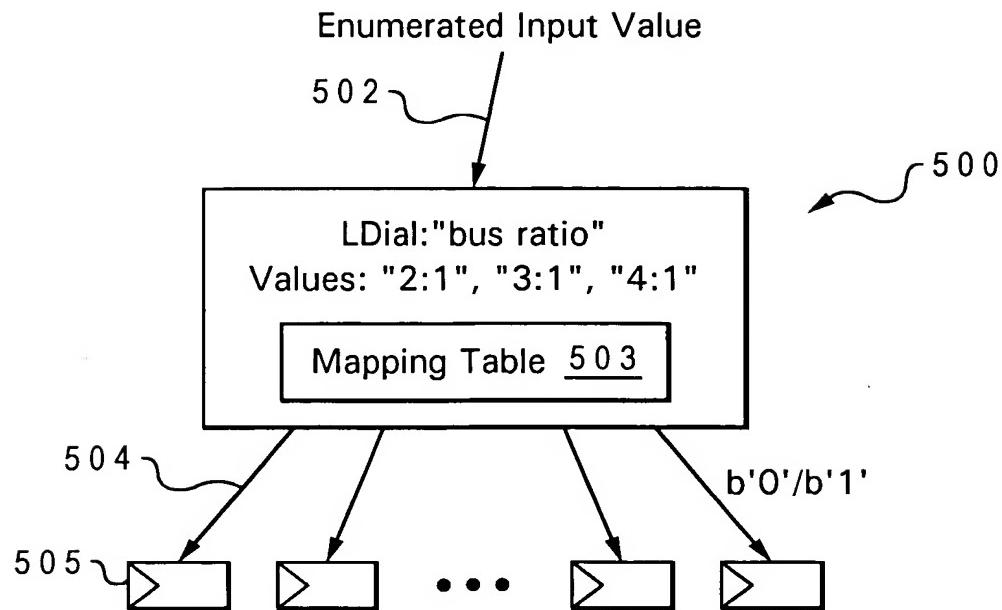


Fig. 5A

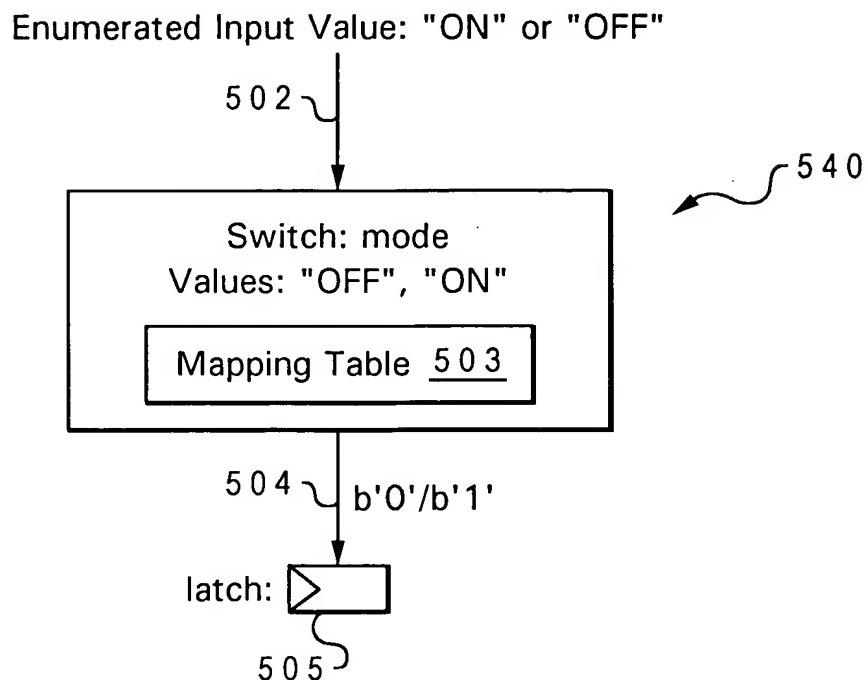
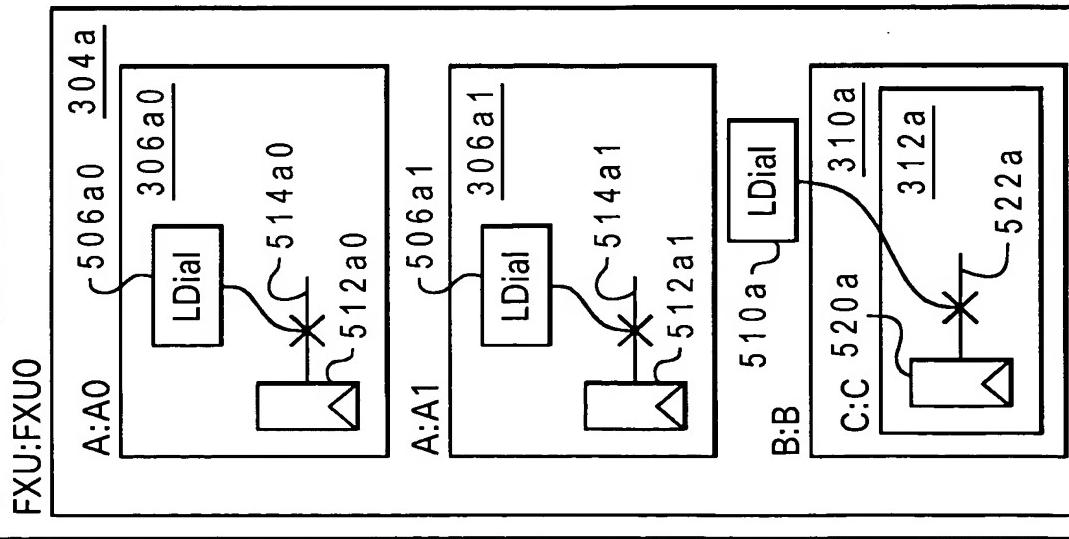


Fig. 5D

TOP:TOP



300'

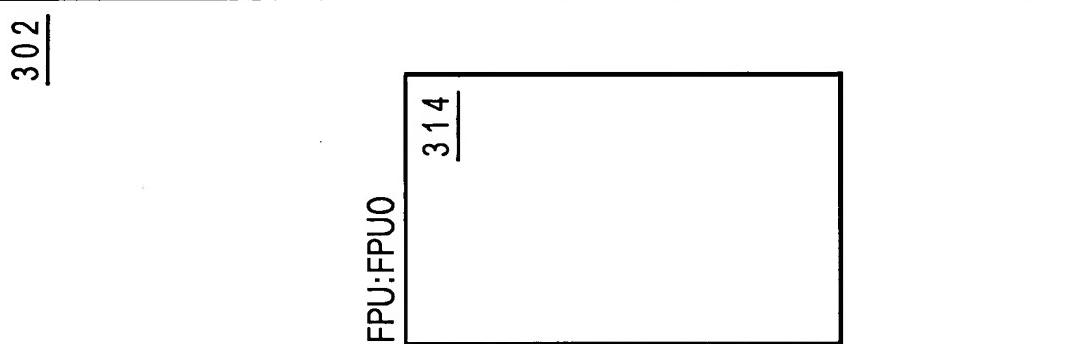
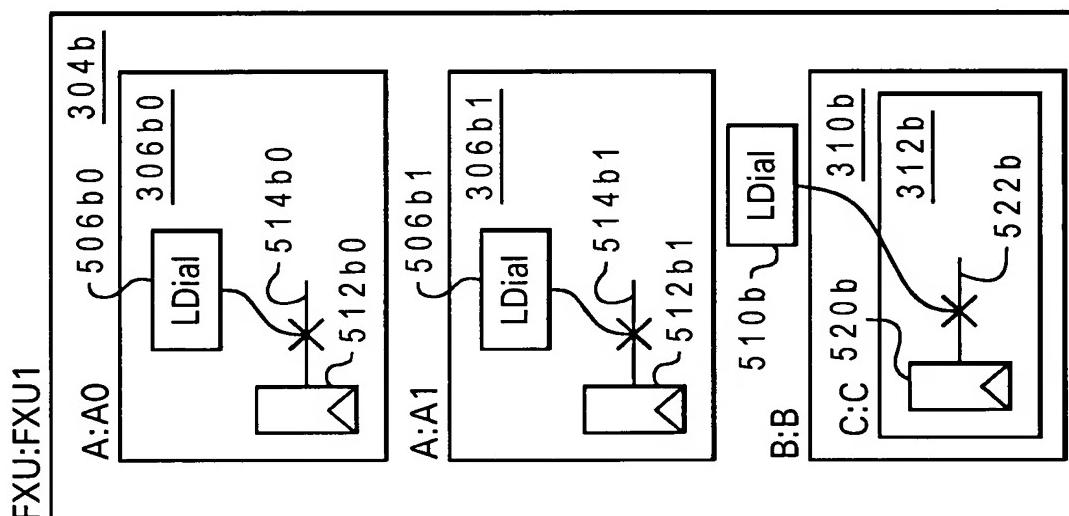
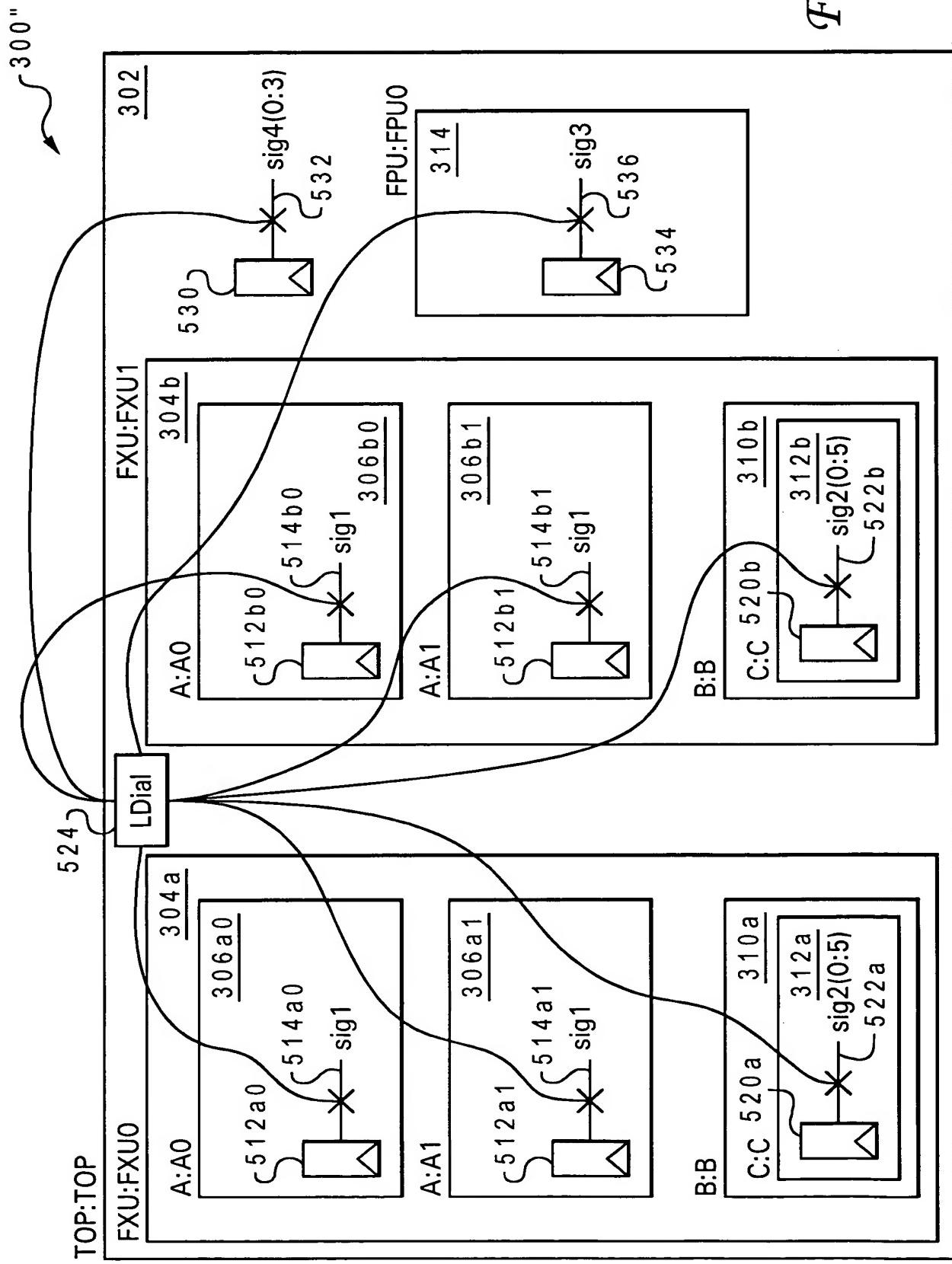


Fig. 5B

Fig. 5C



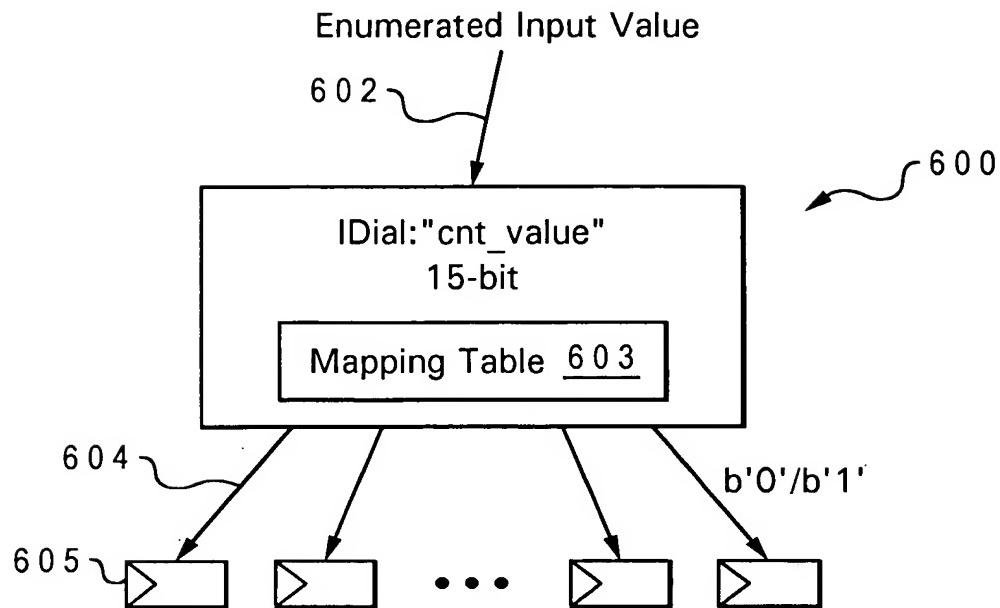


Fig. 6A

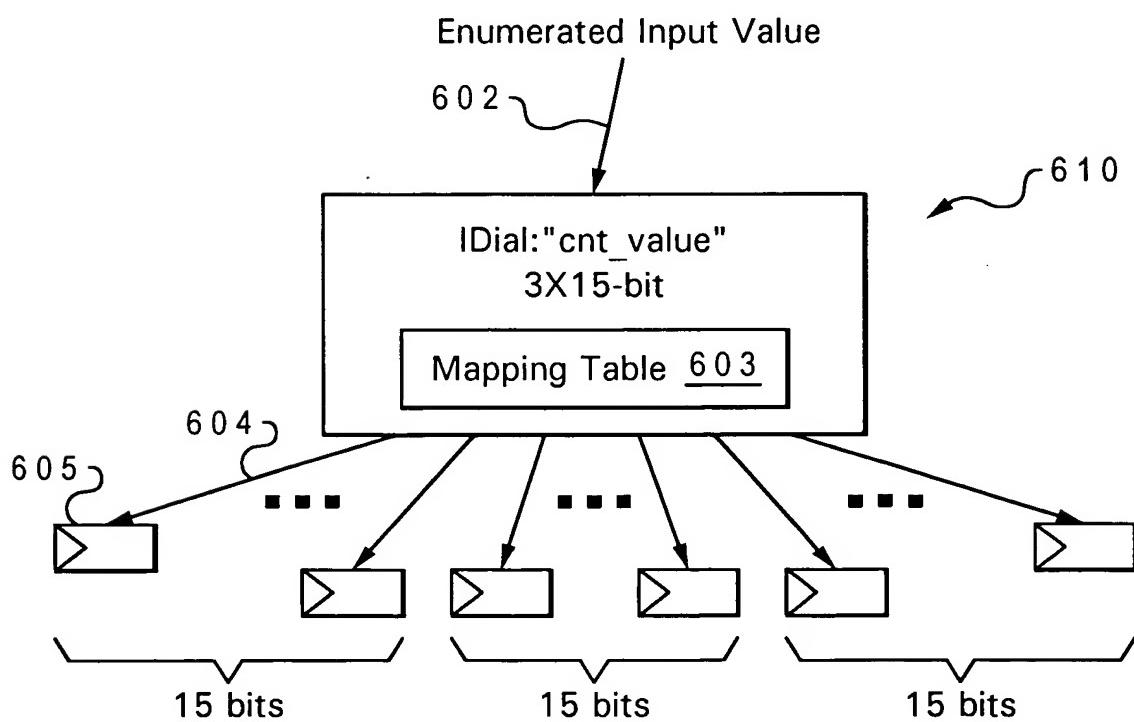


Fig. 6B

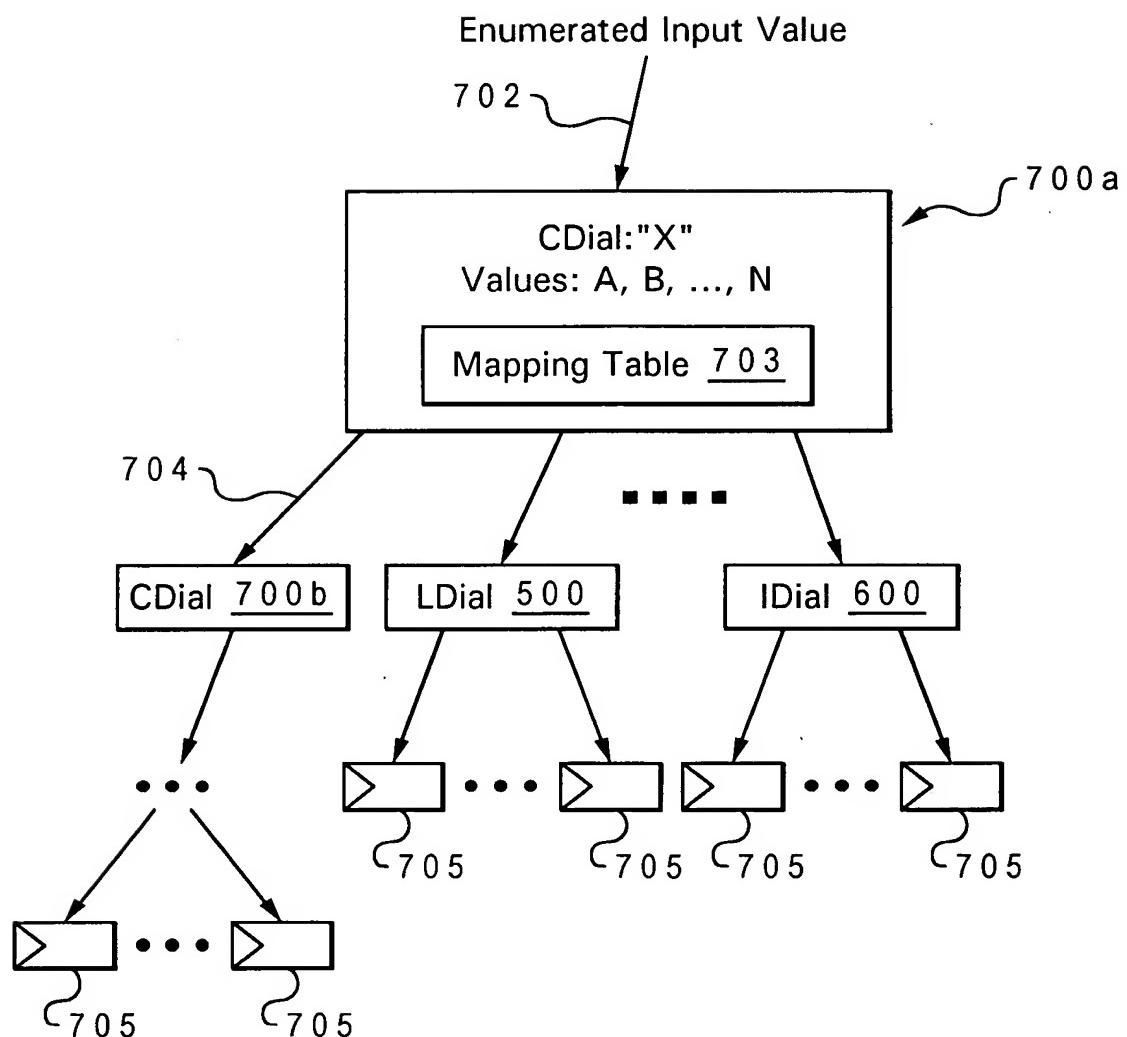
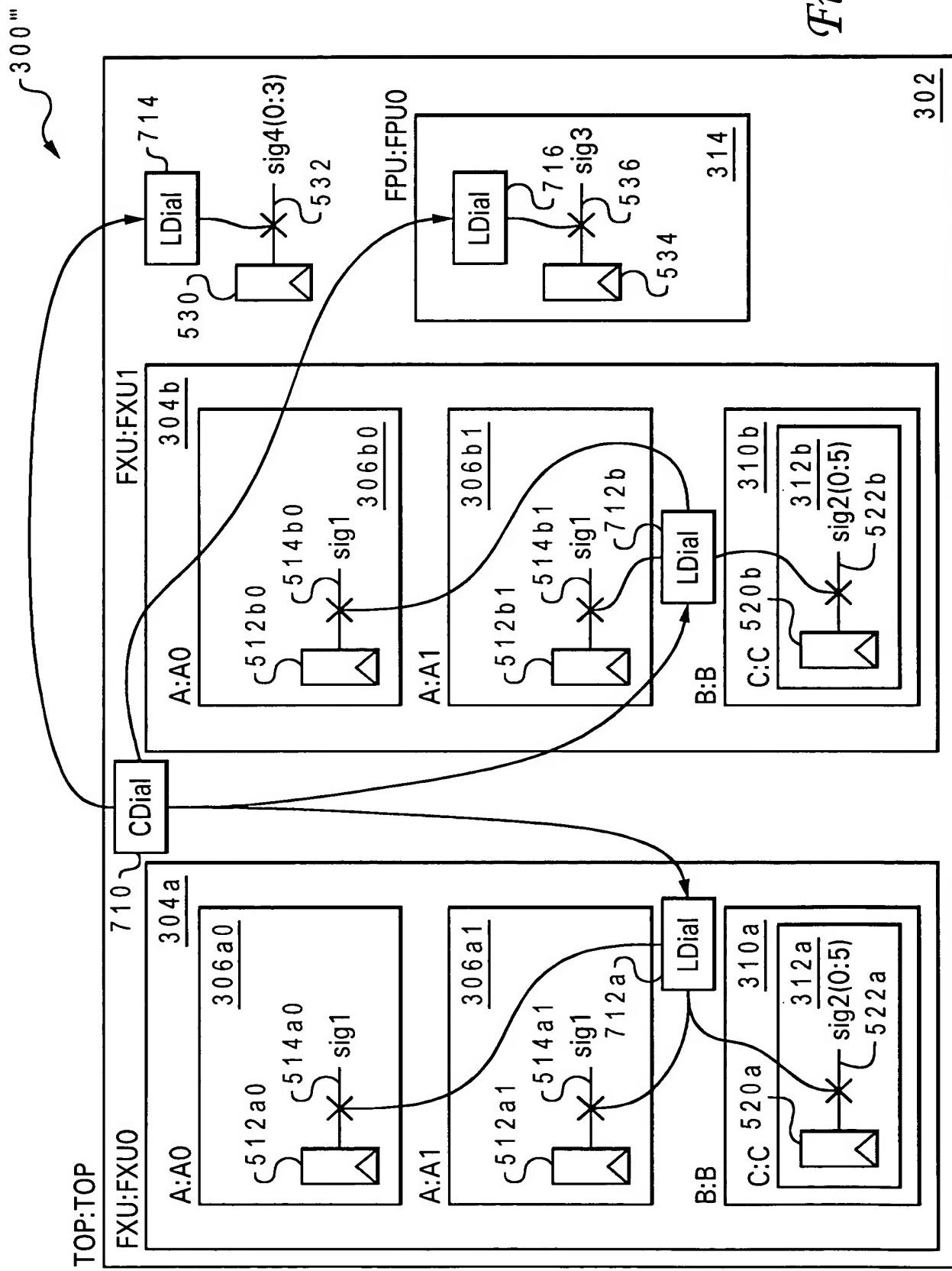


Fig. 7A



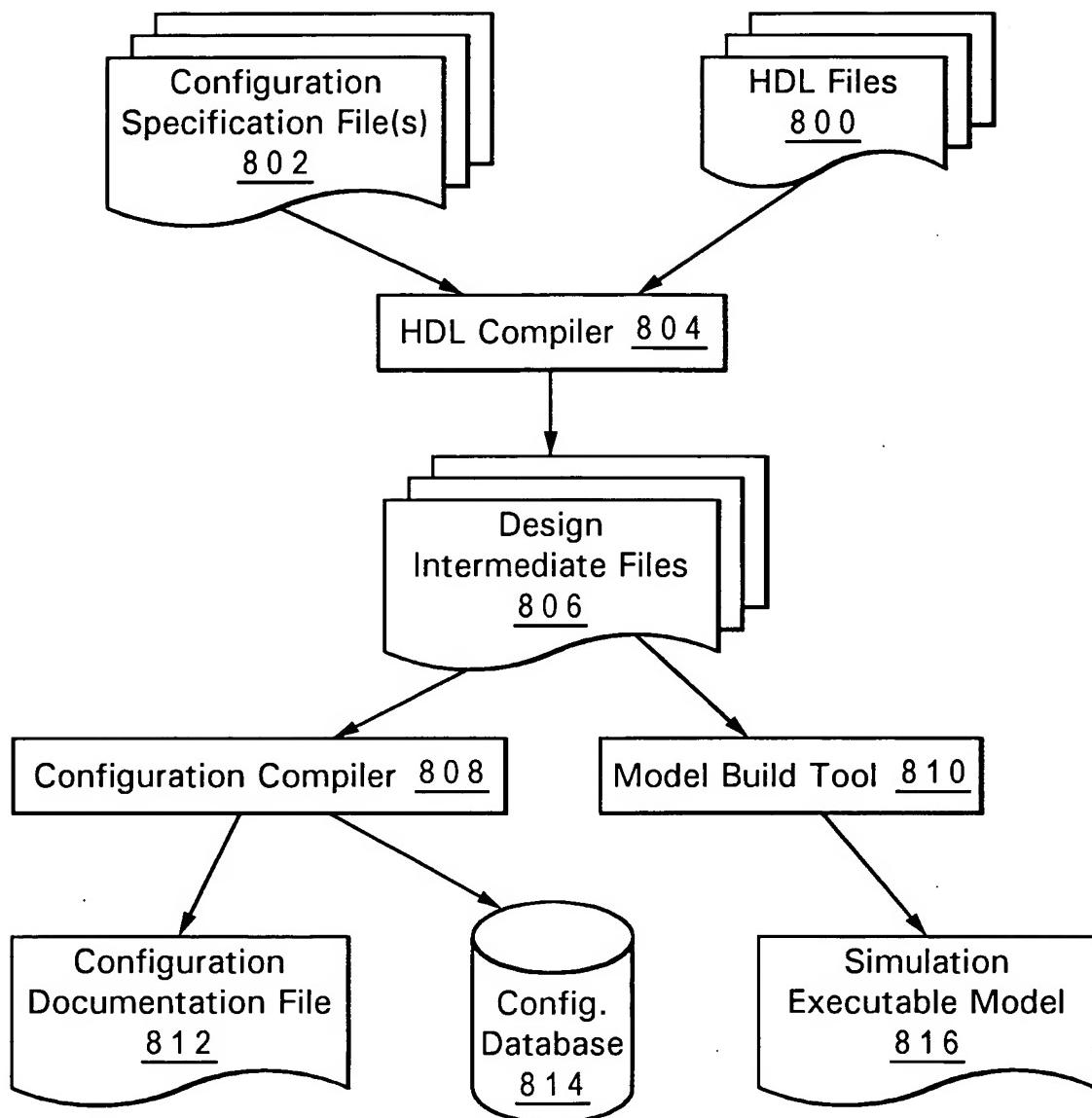


Fig. 8

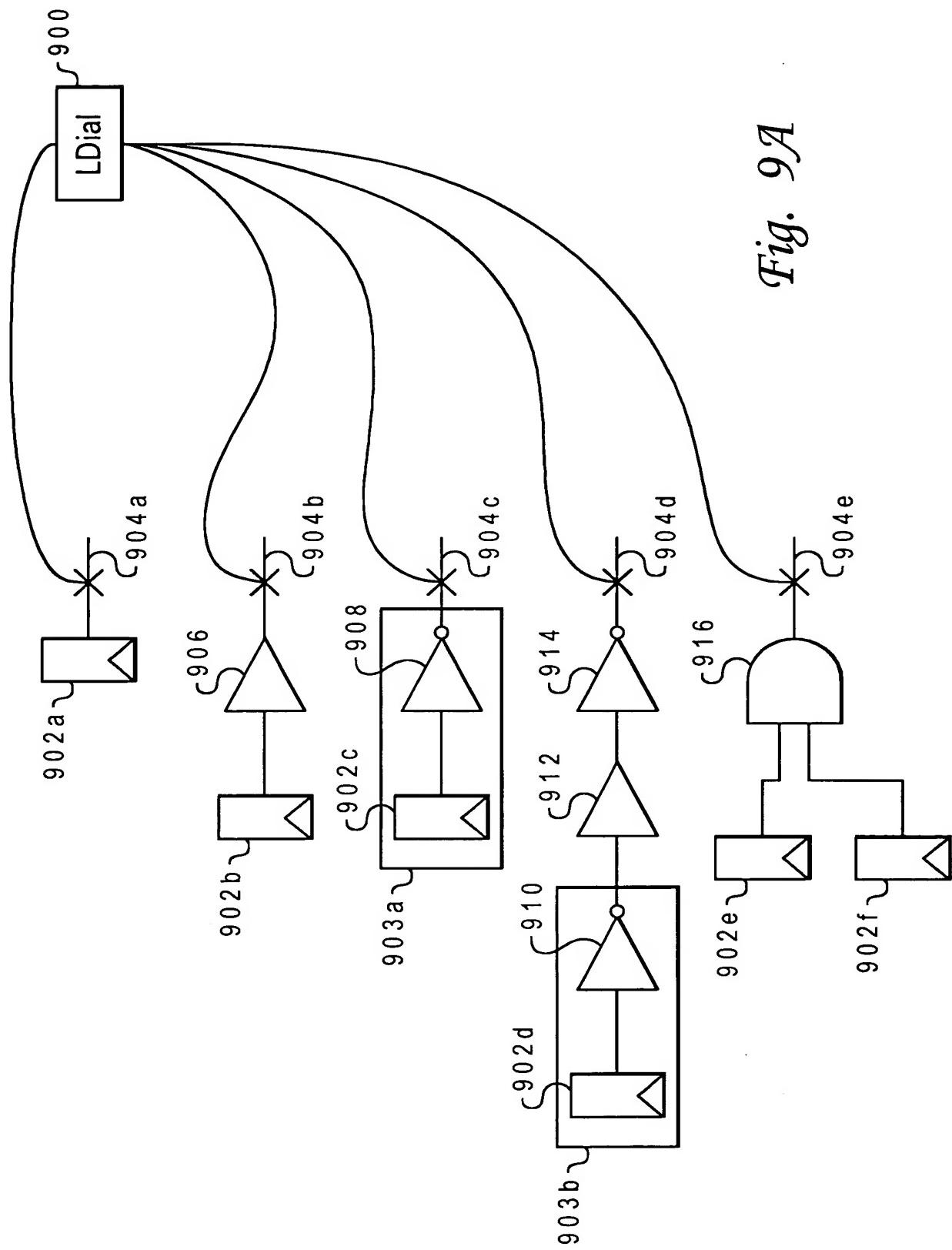


Fig. 9A

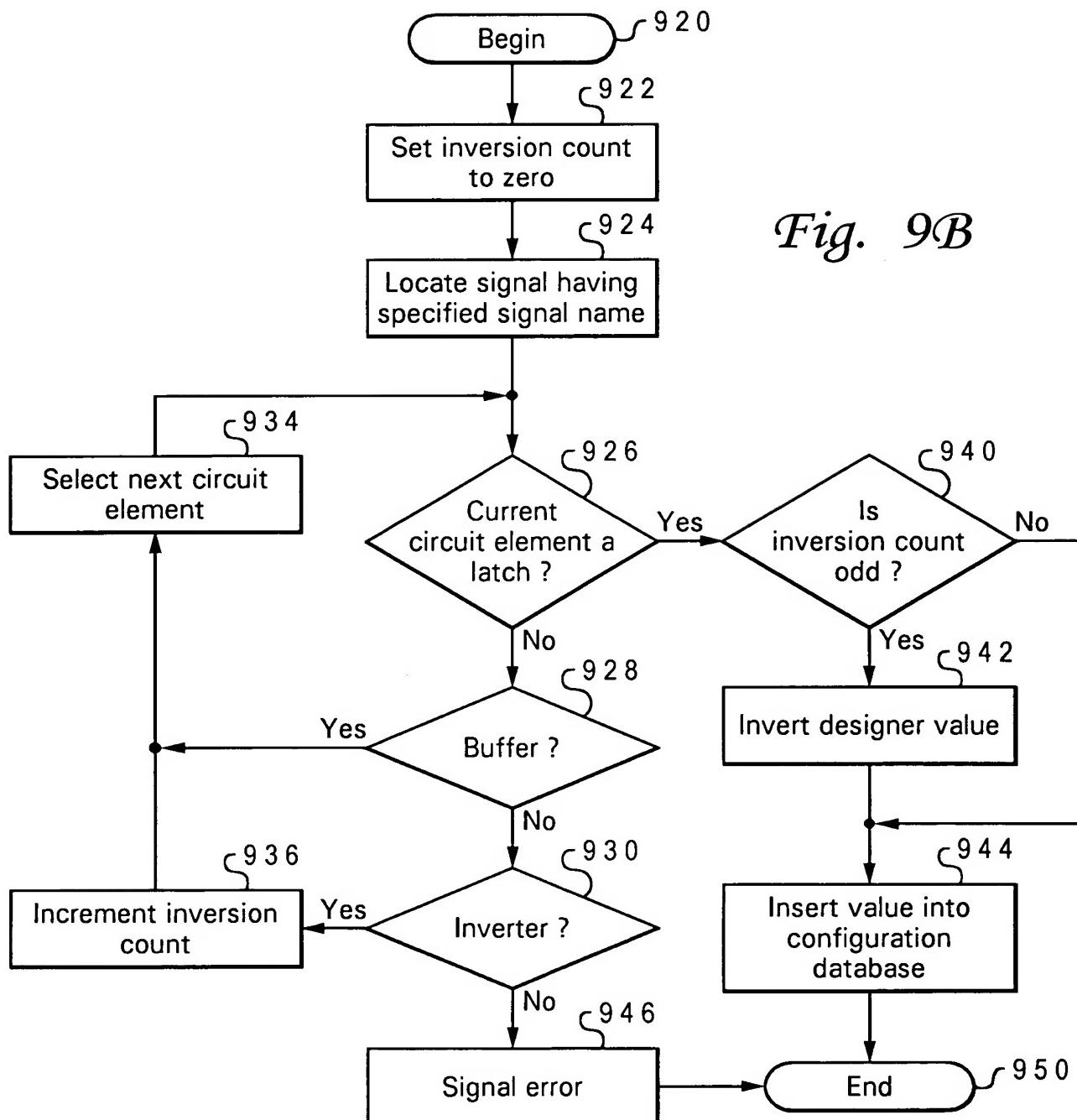
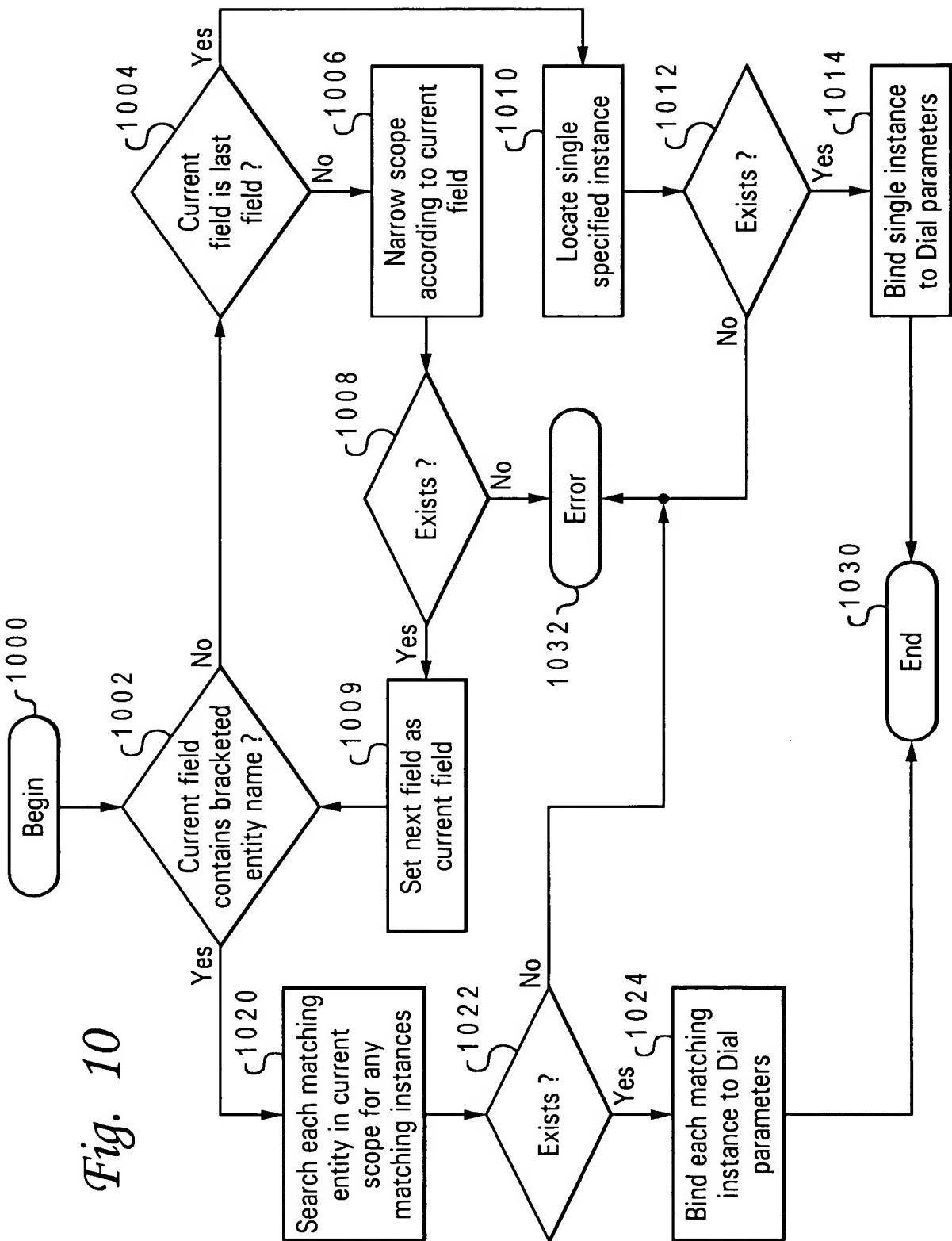


Fig. 9B



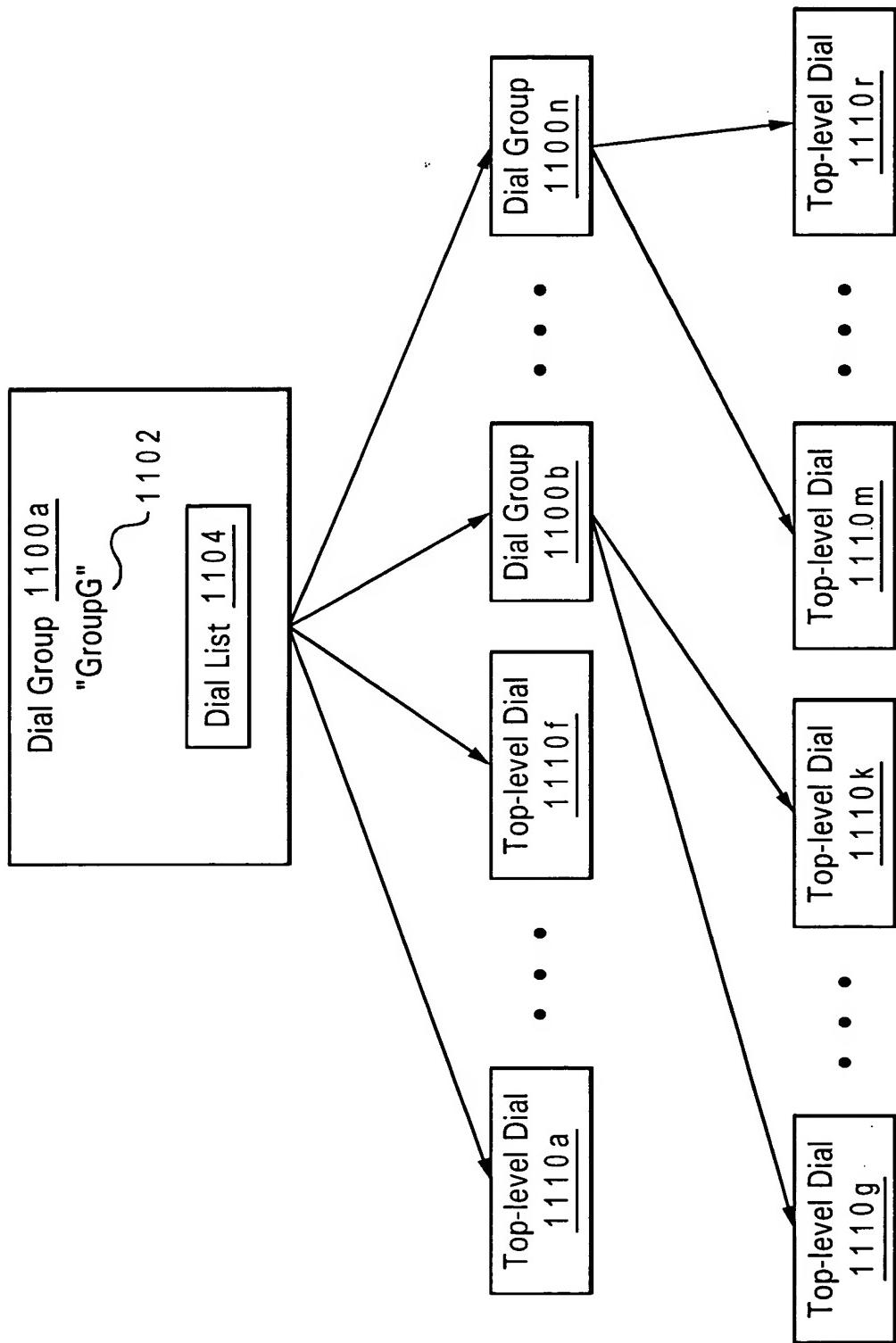


Fig. 11A

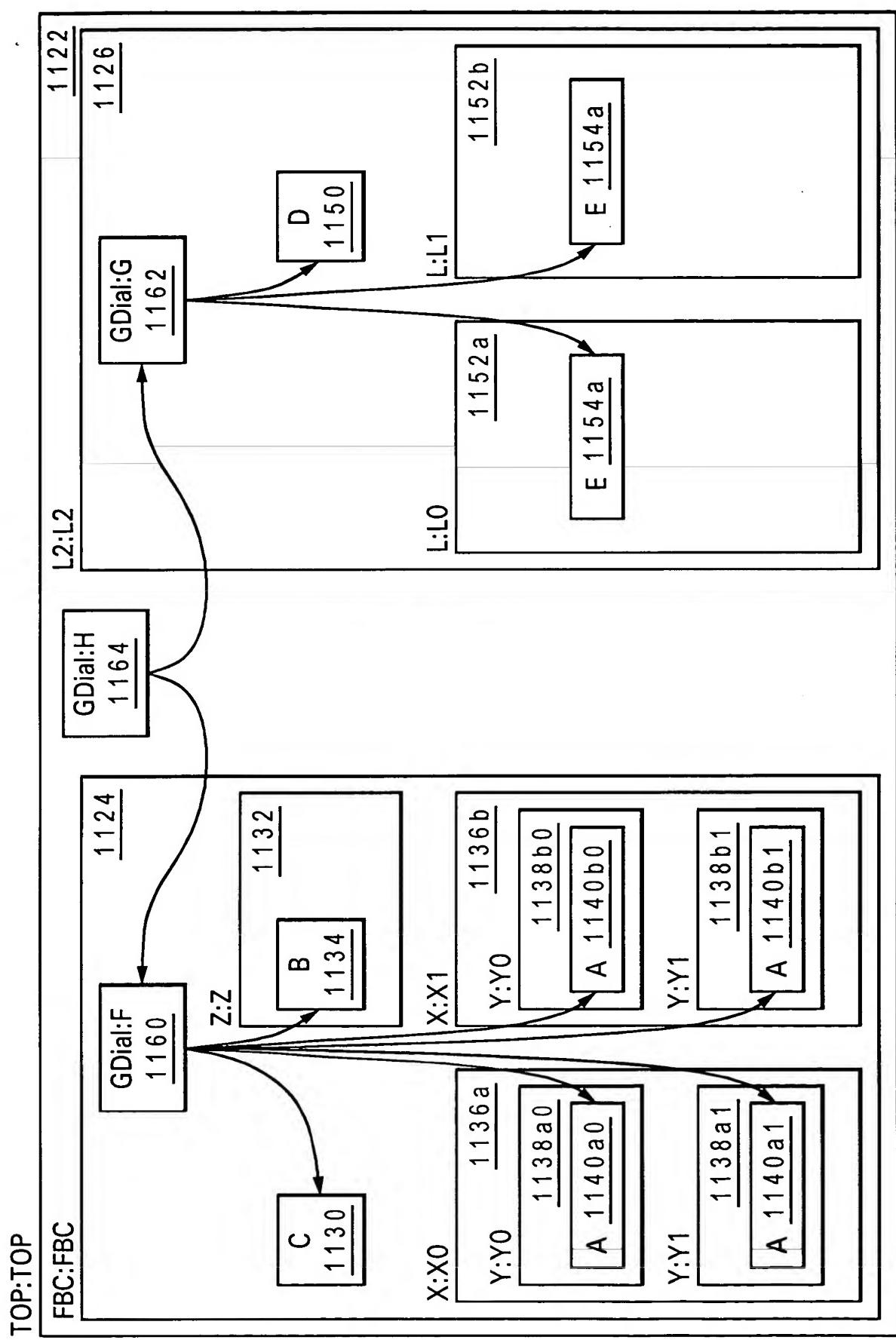
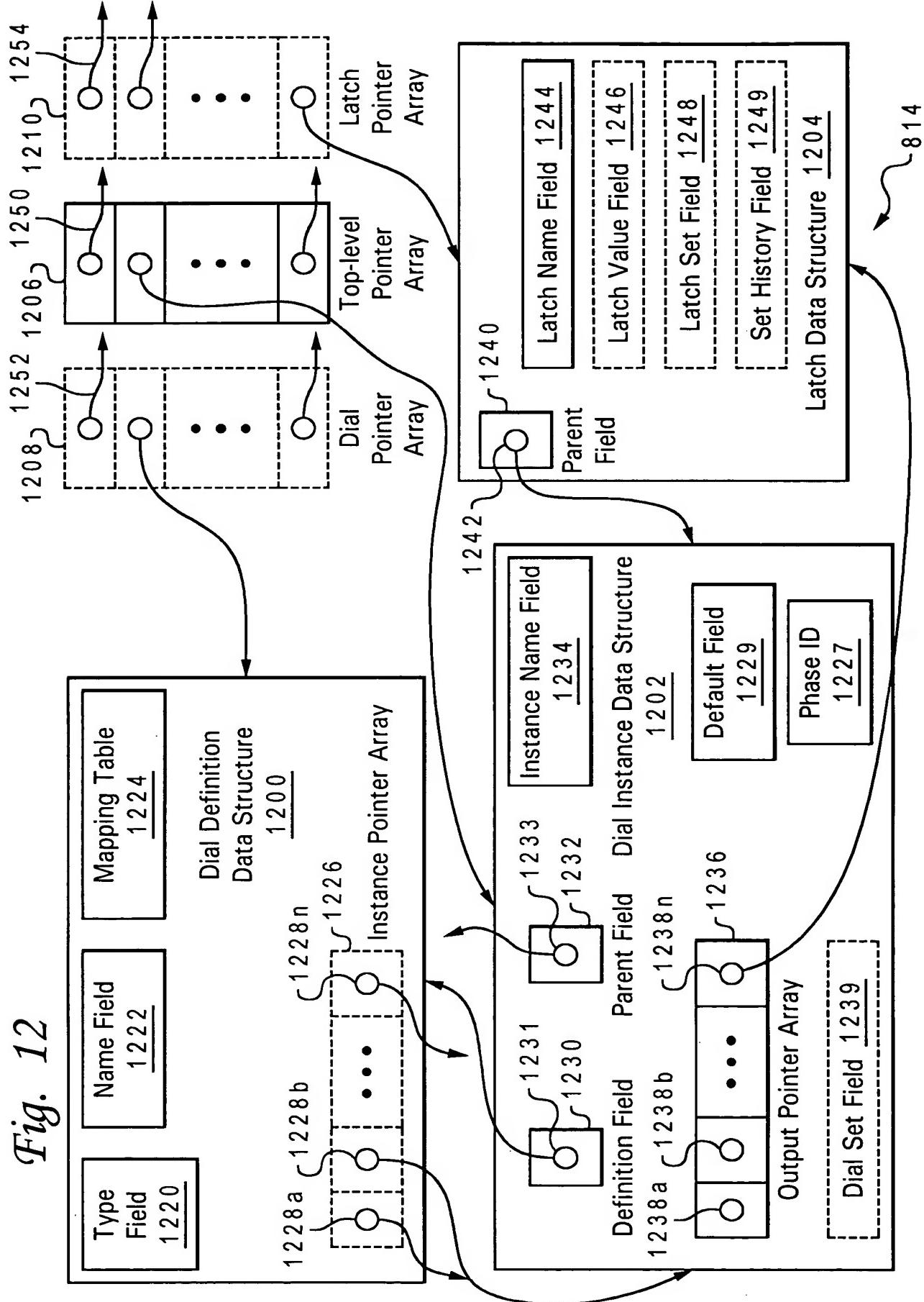


Fig. 11B
1120

Fig. 12



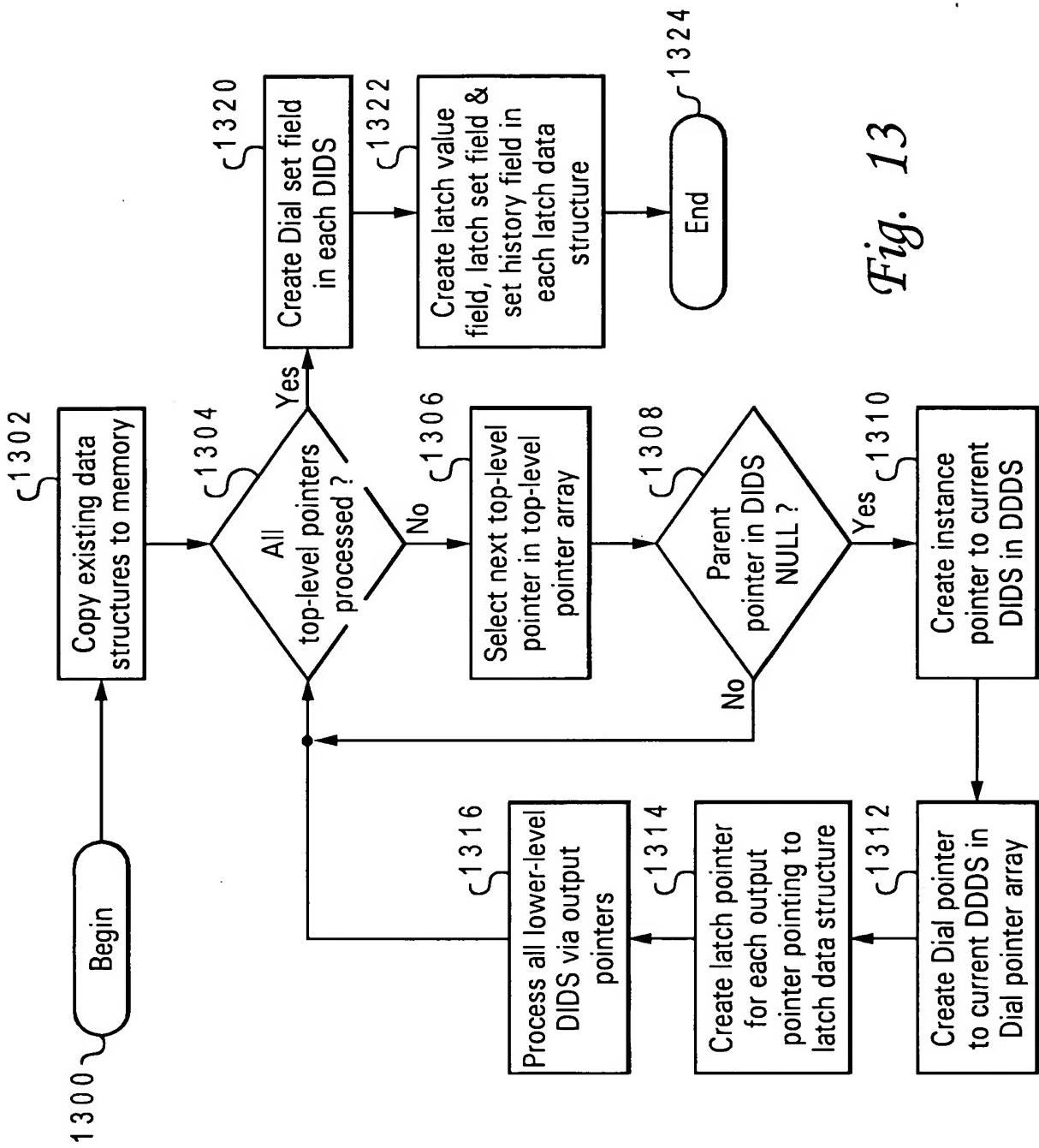


Fig. 13

Fig. 14

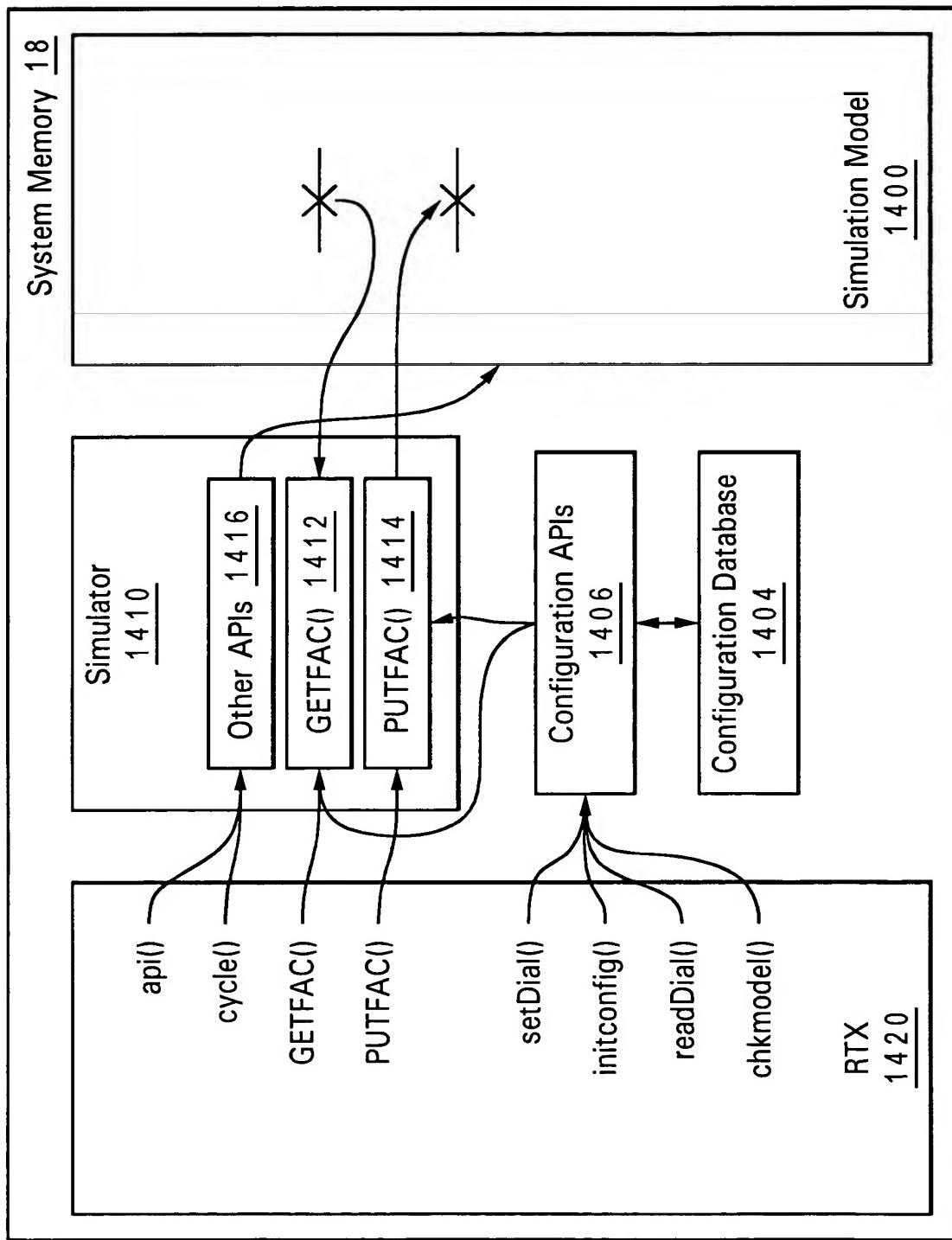


Fig. 15

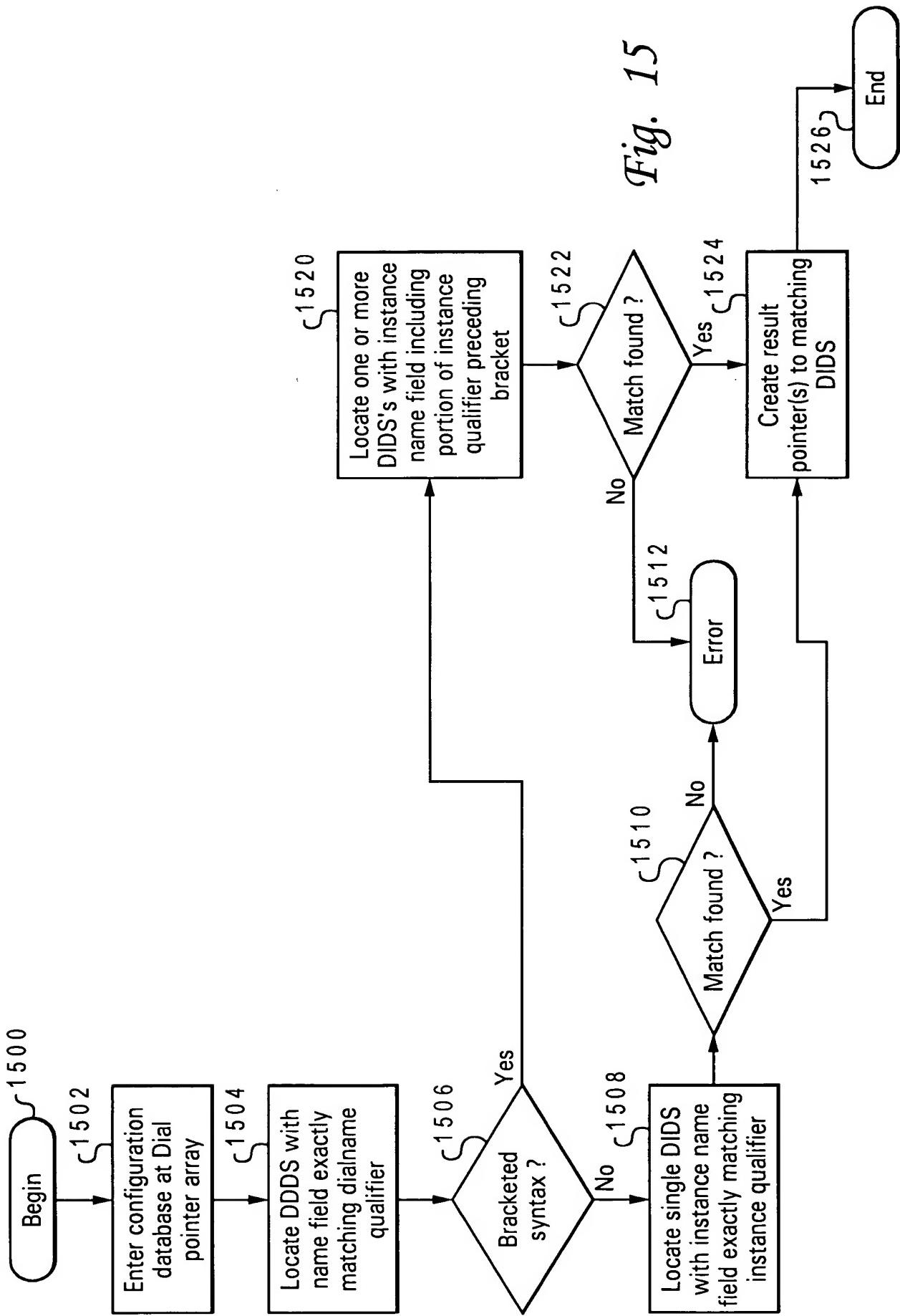
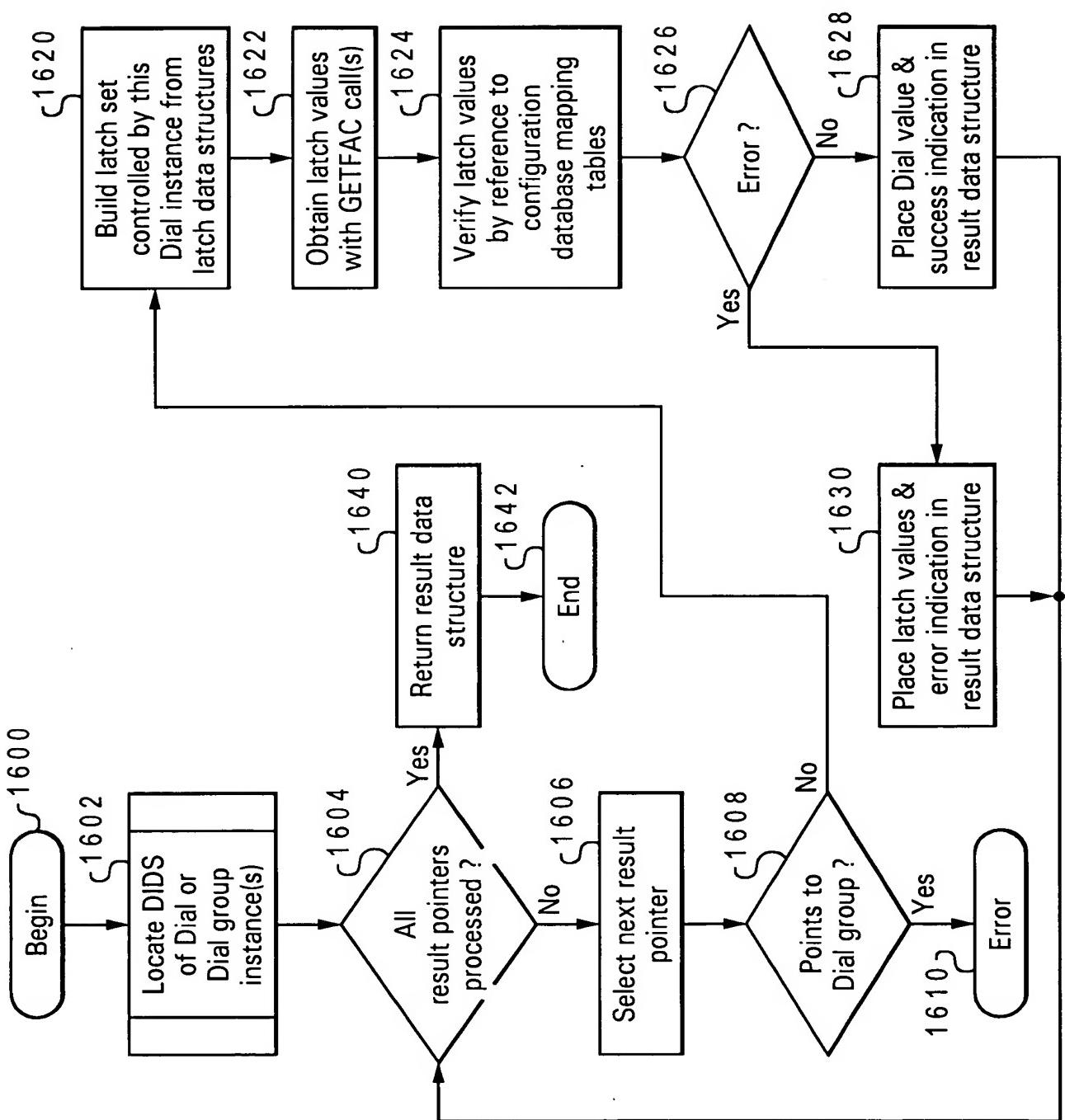


Fig. 16A



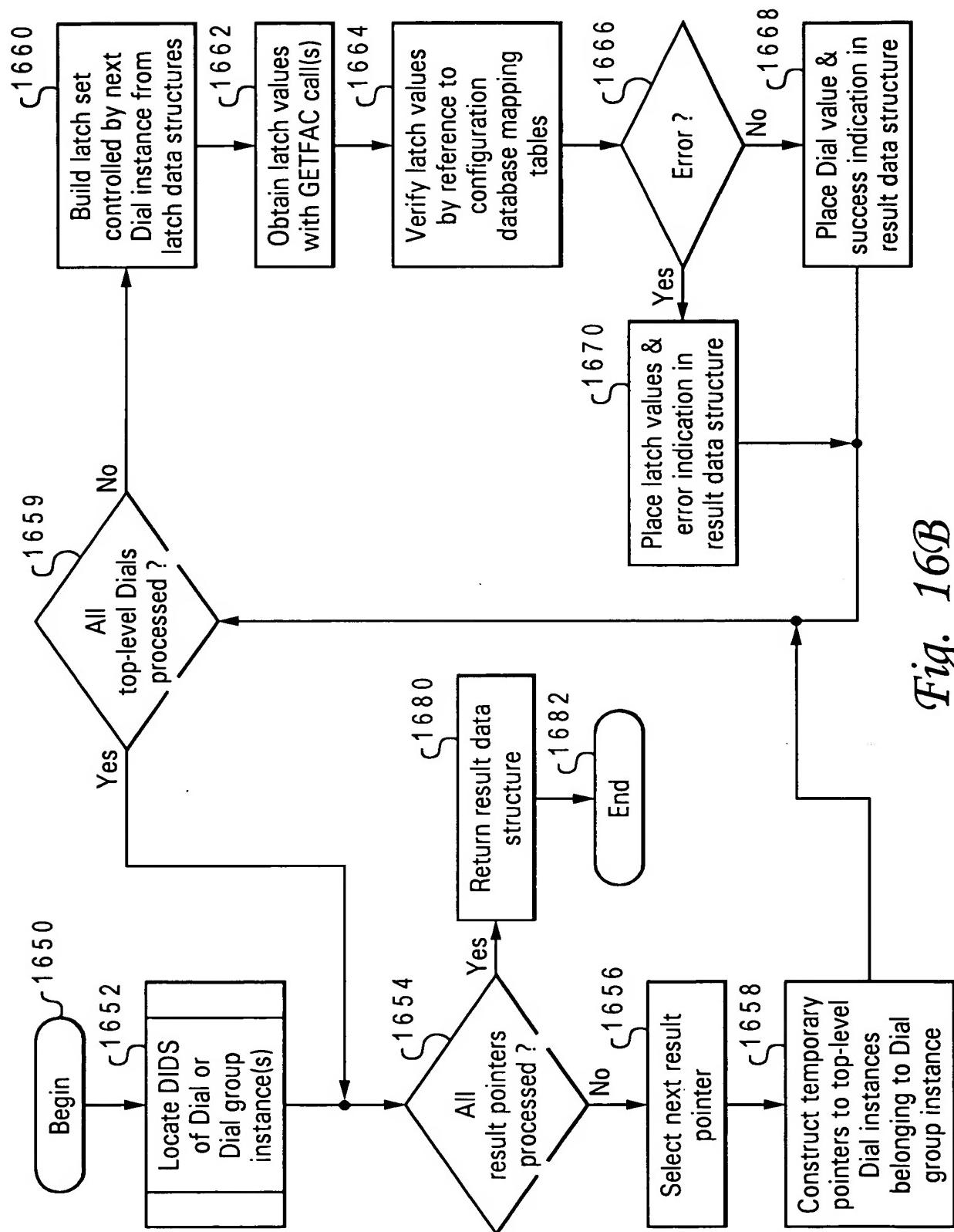


Fig. 16B

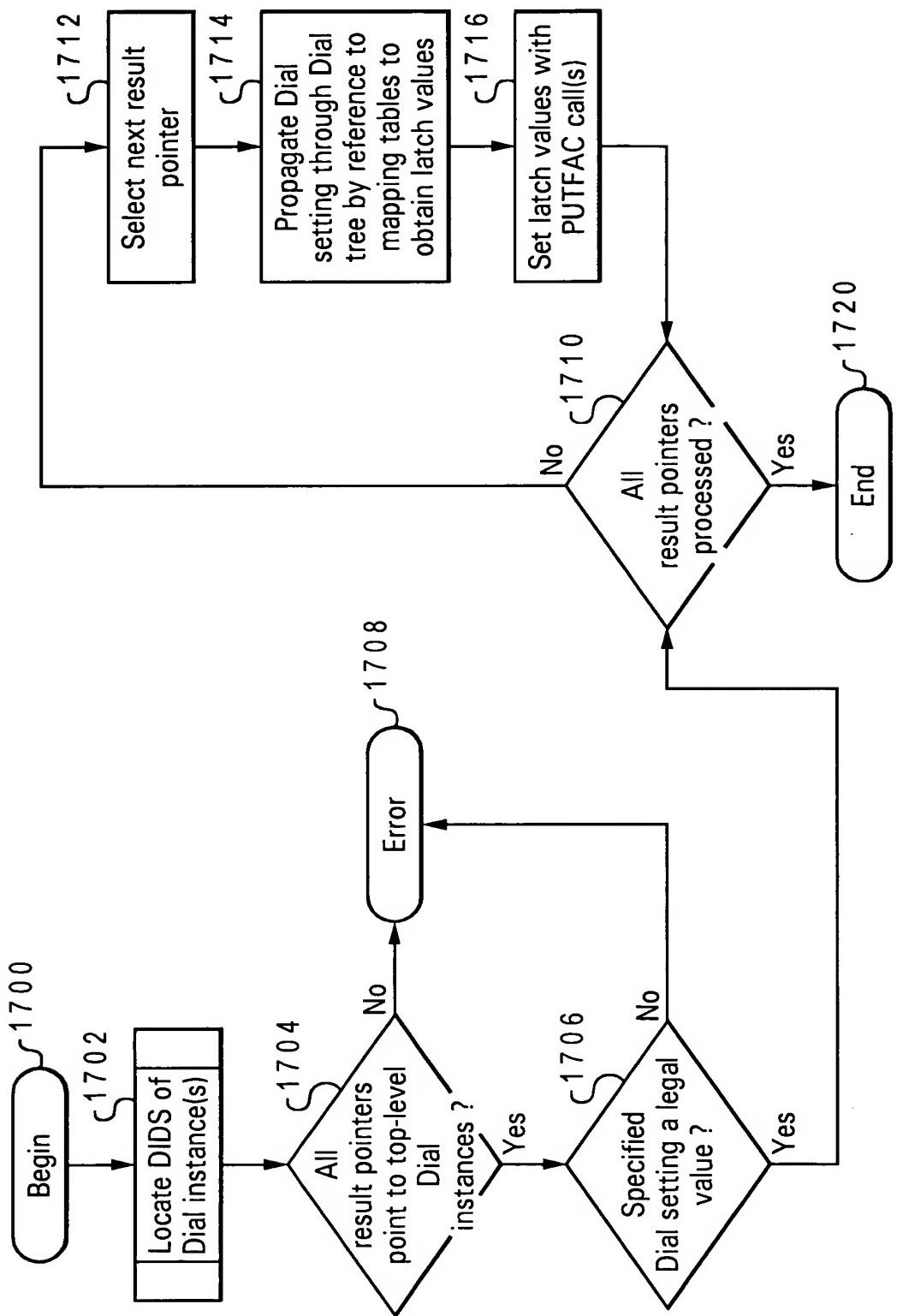


Fig. 17A

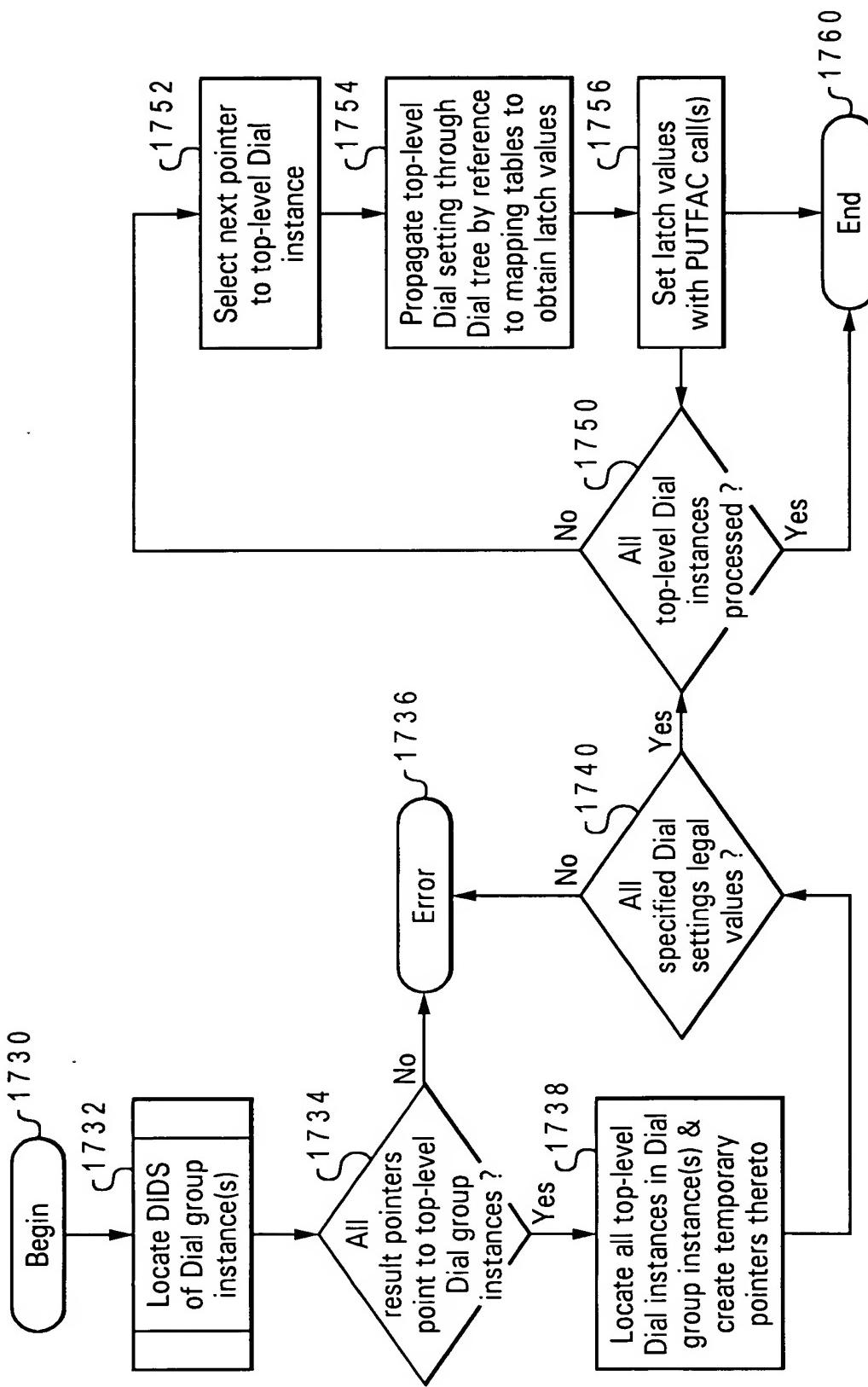


Fig. 17B

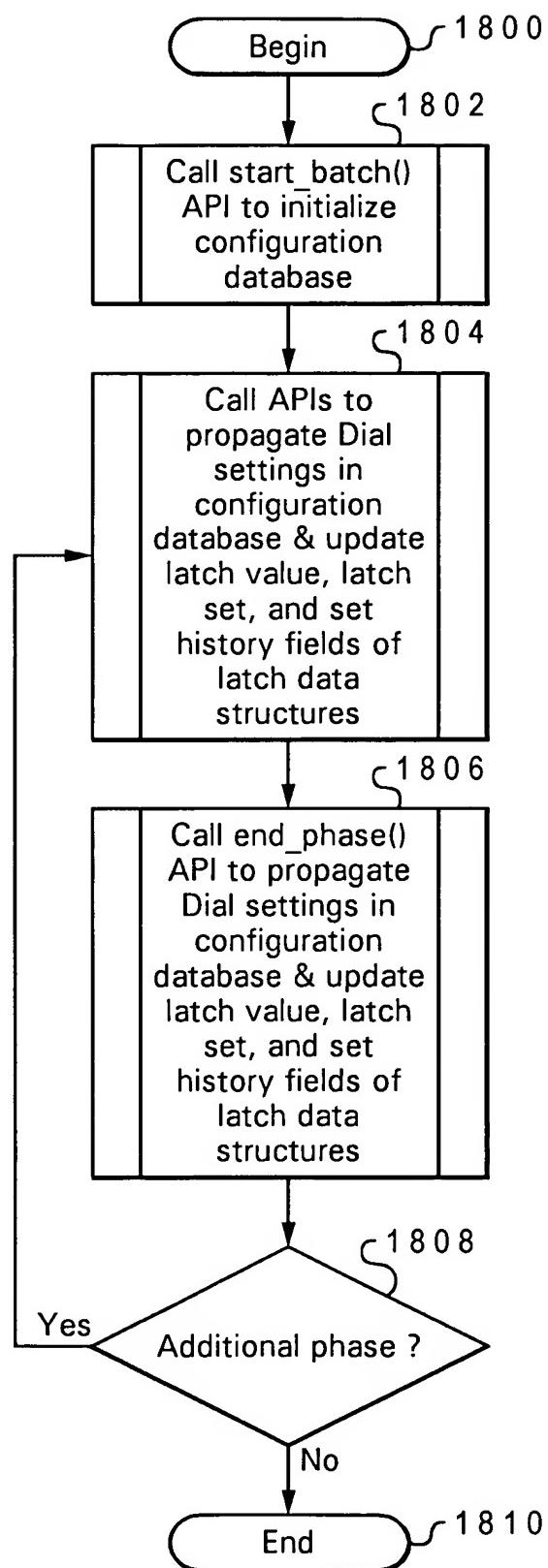


Fig. 18A

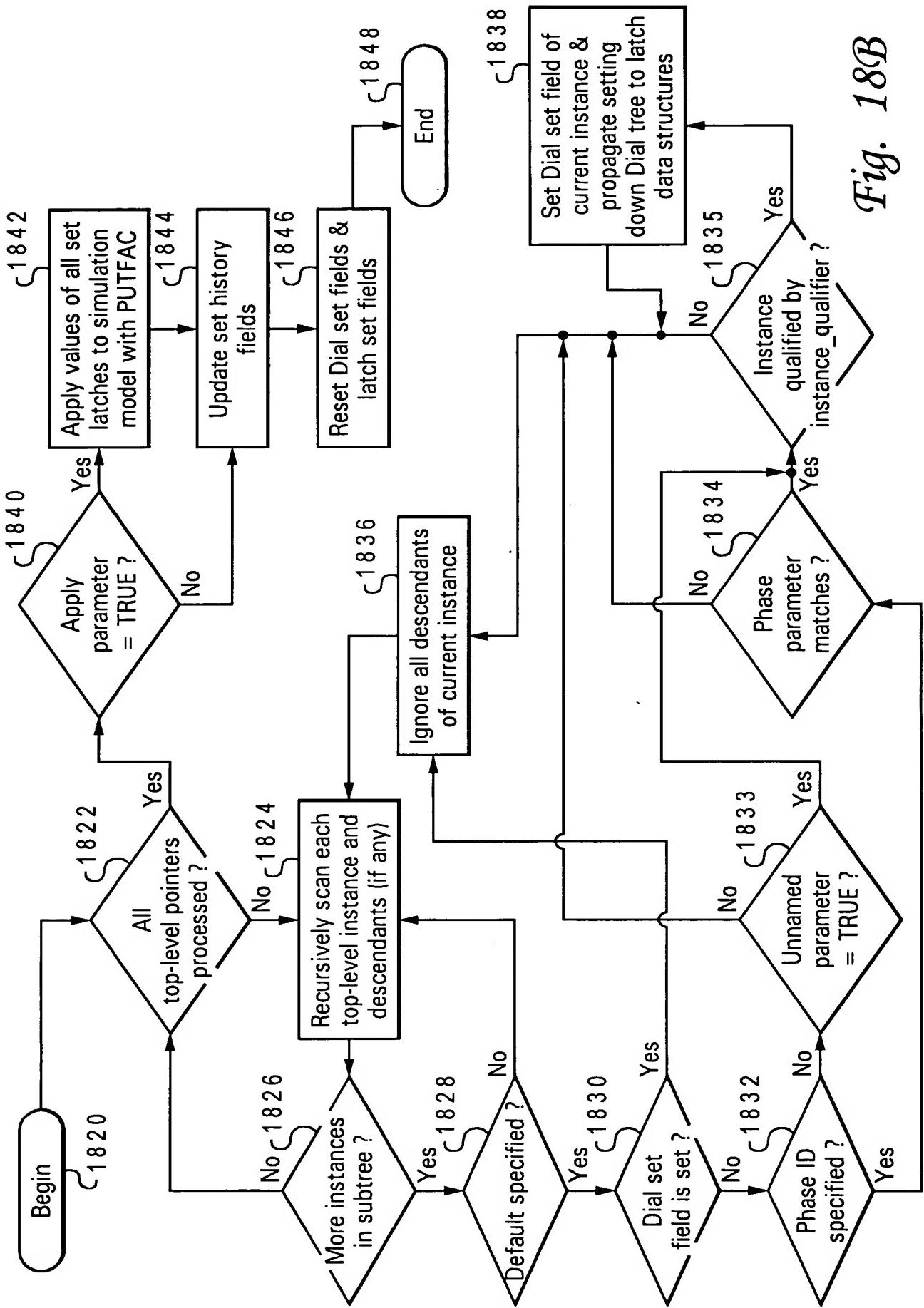
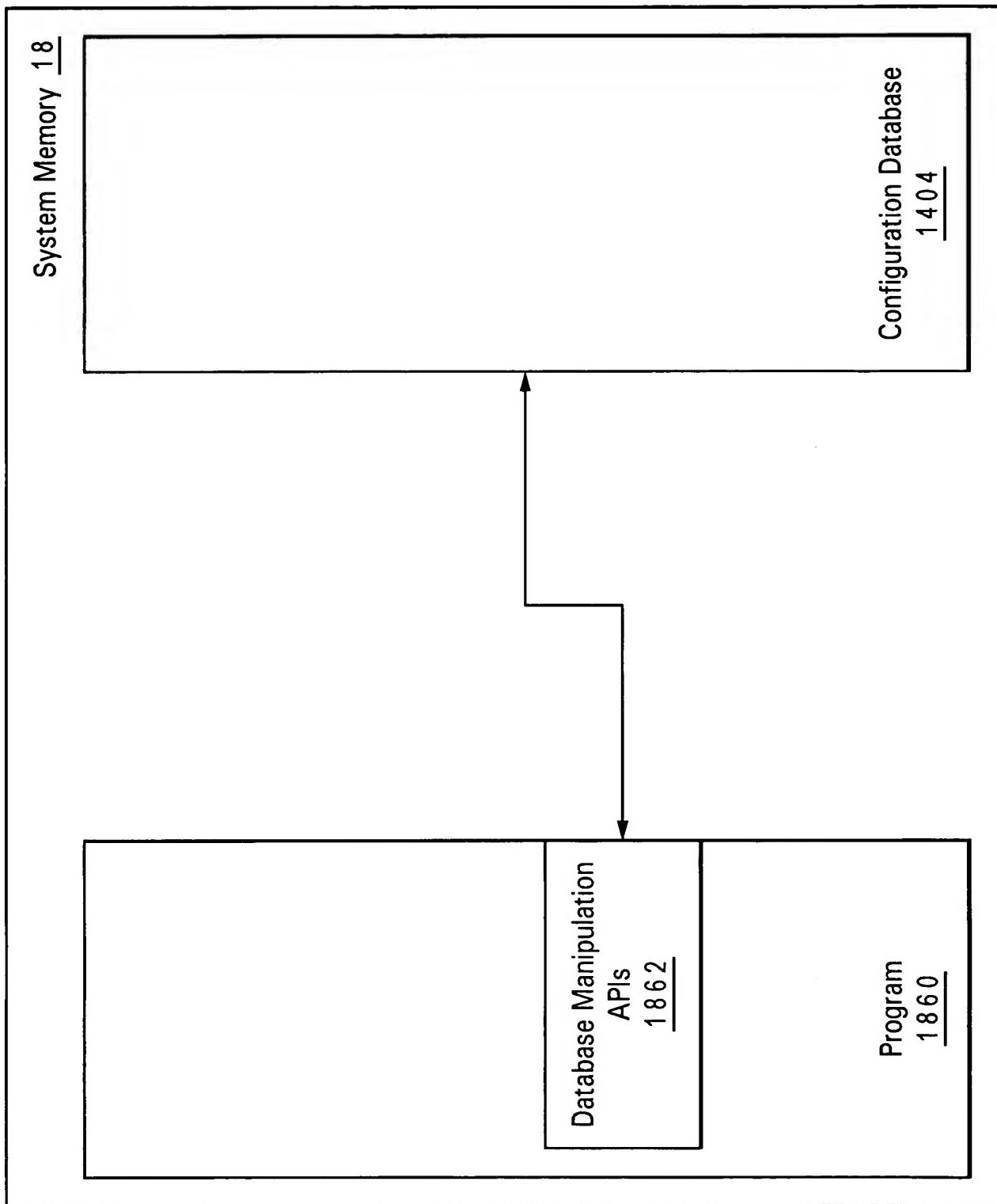


Fig. 18B

Fig. 18C



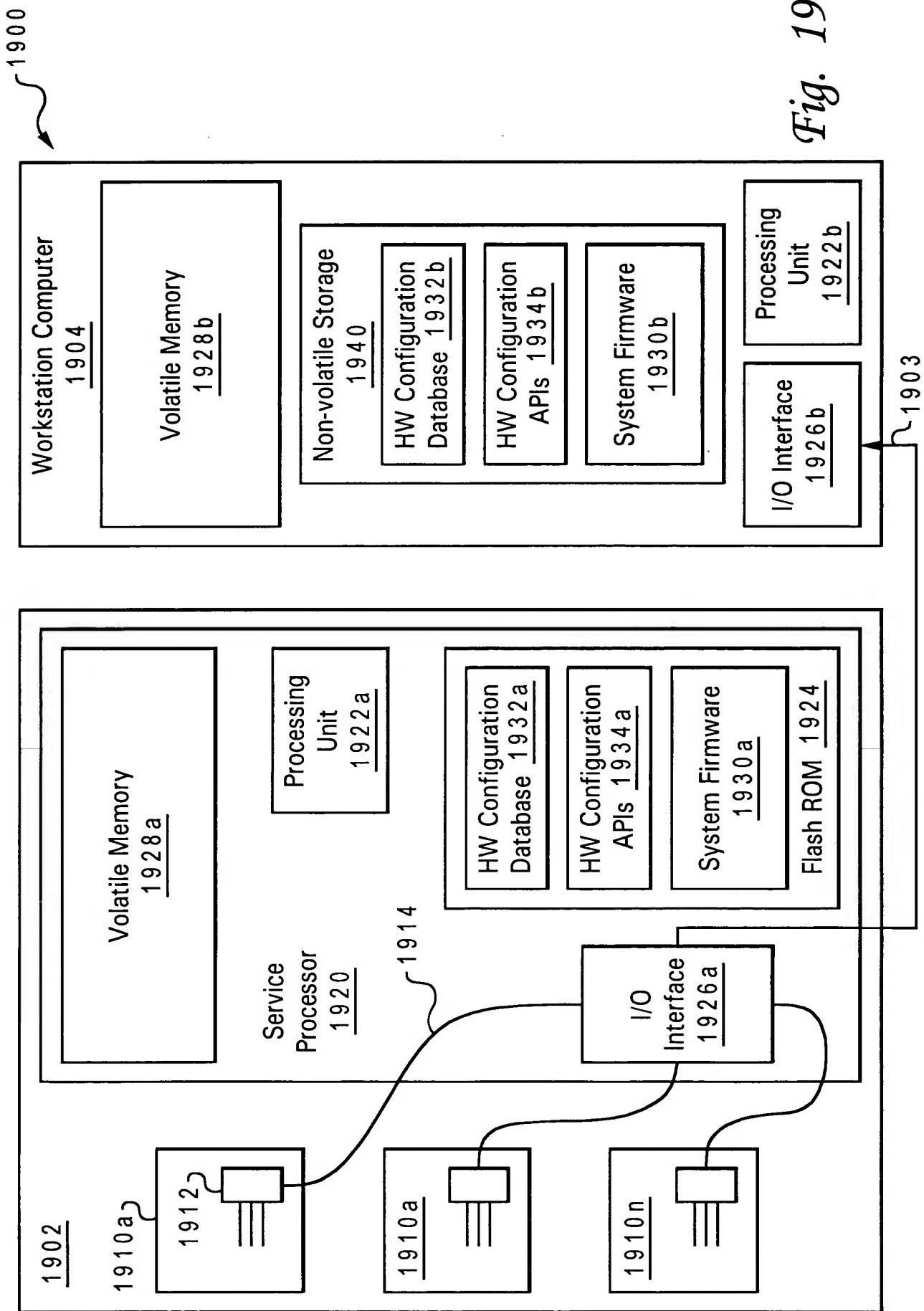
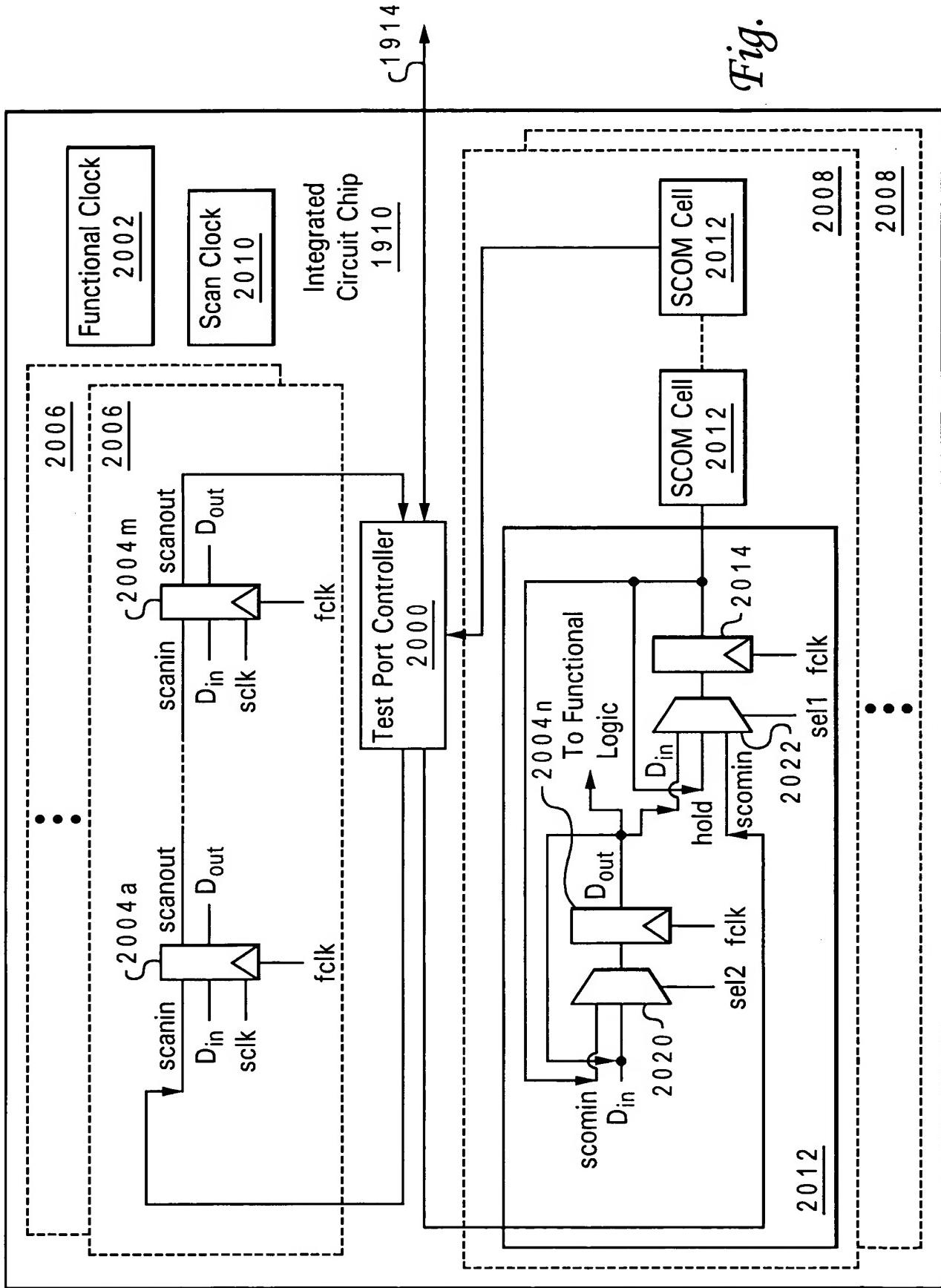


Fig. 20



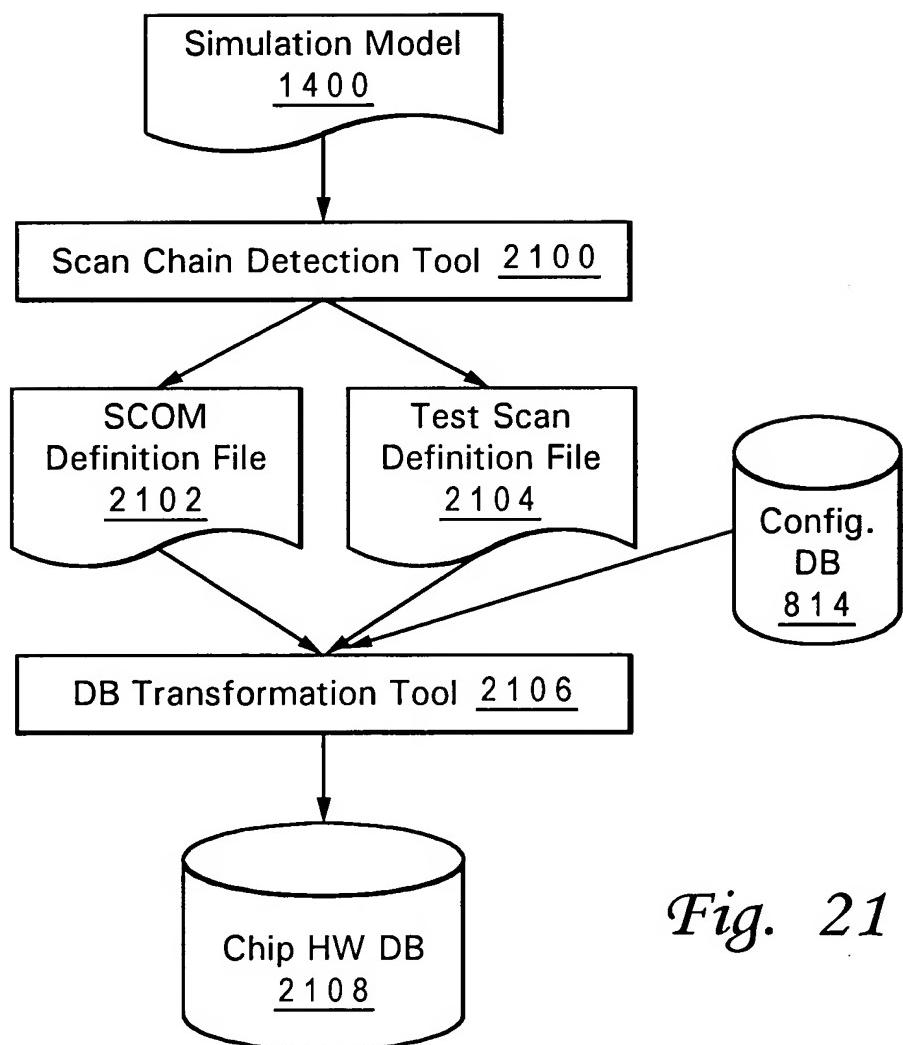
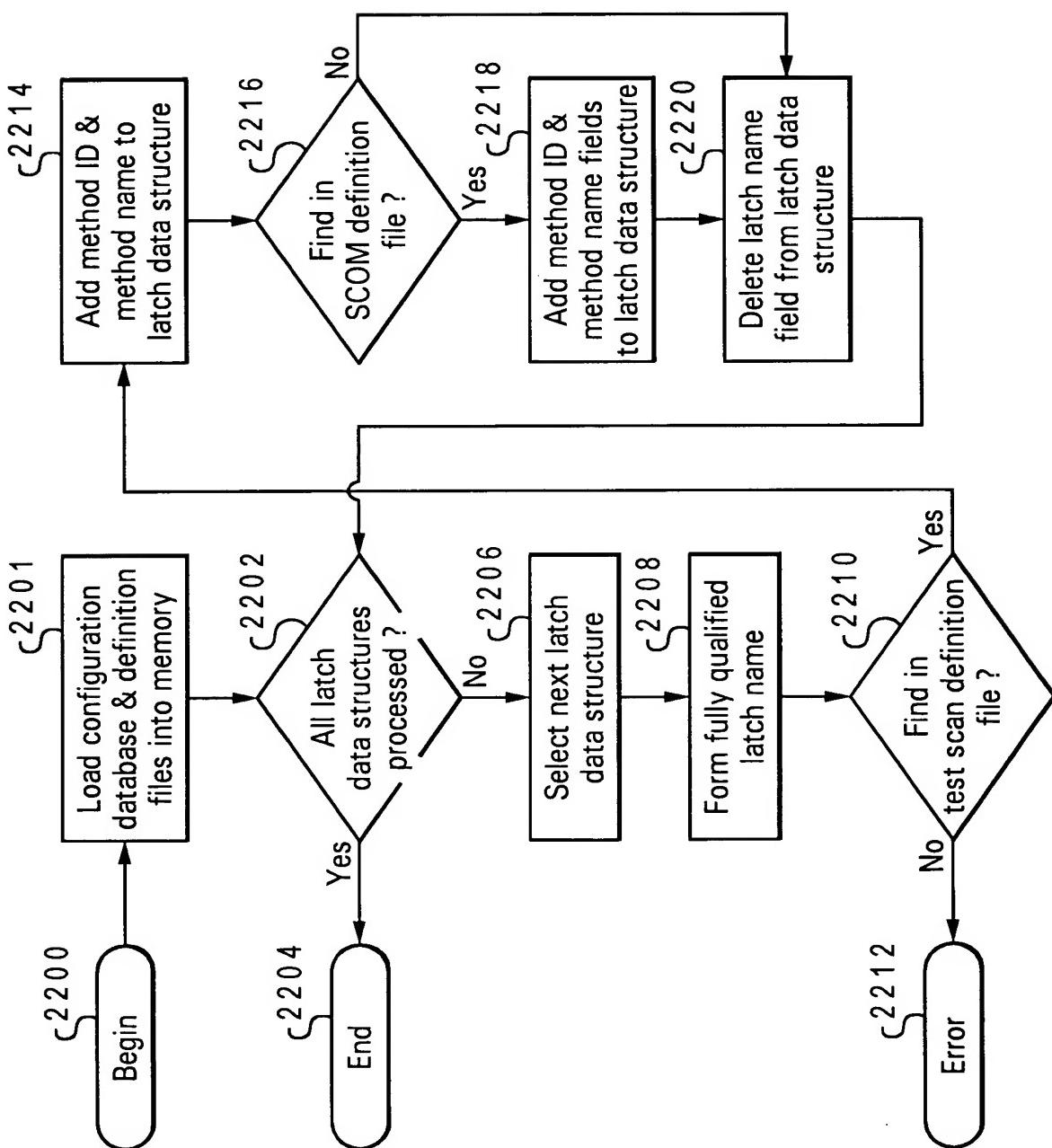


Fig. 21

Fig. 22A



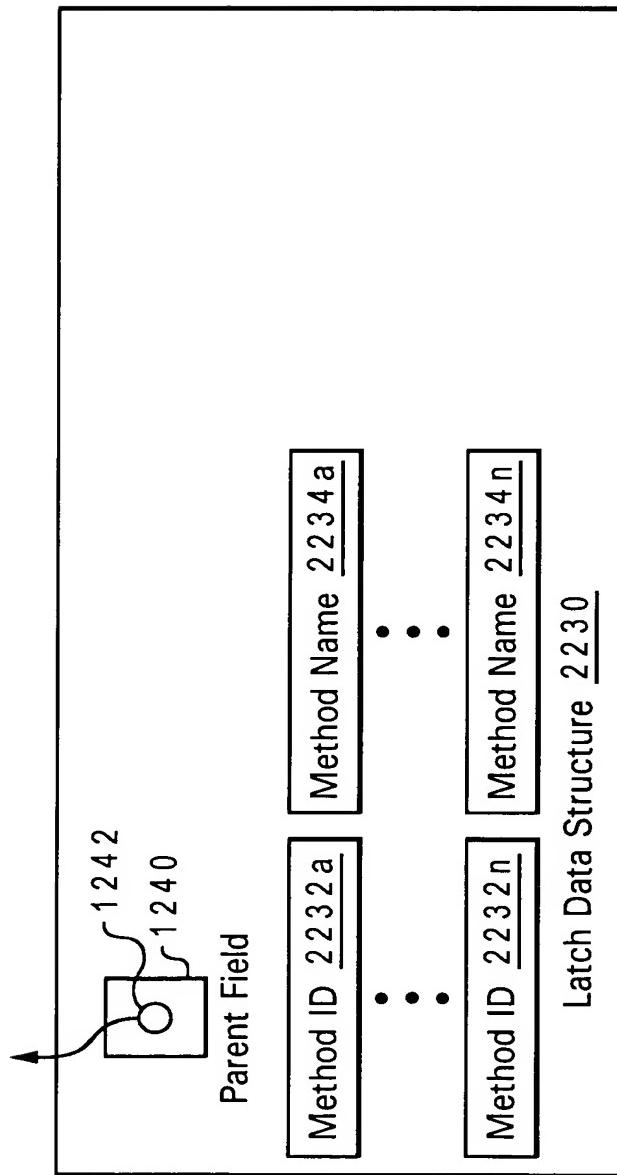


Fig. 22B

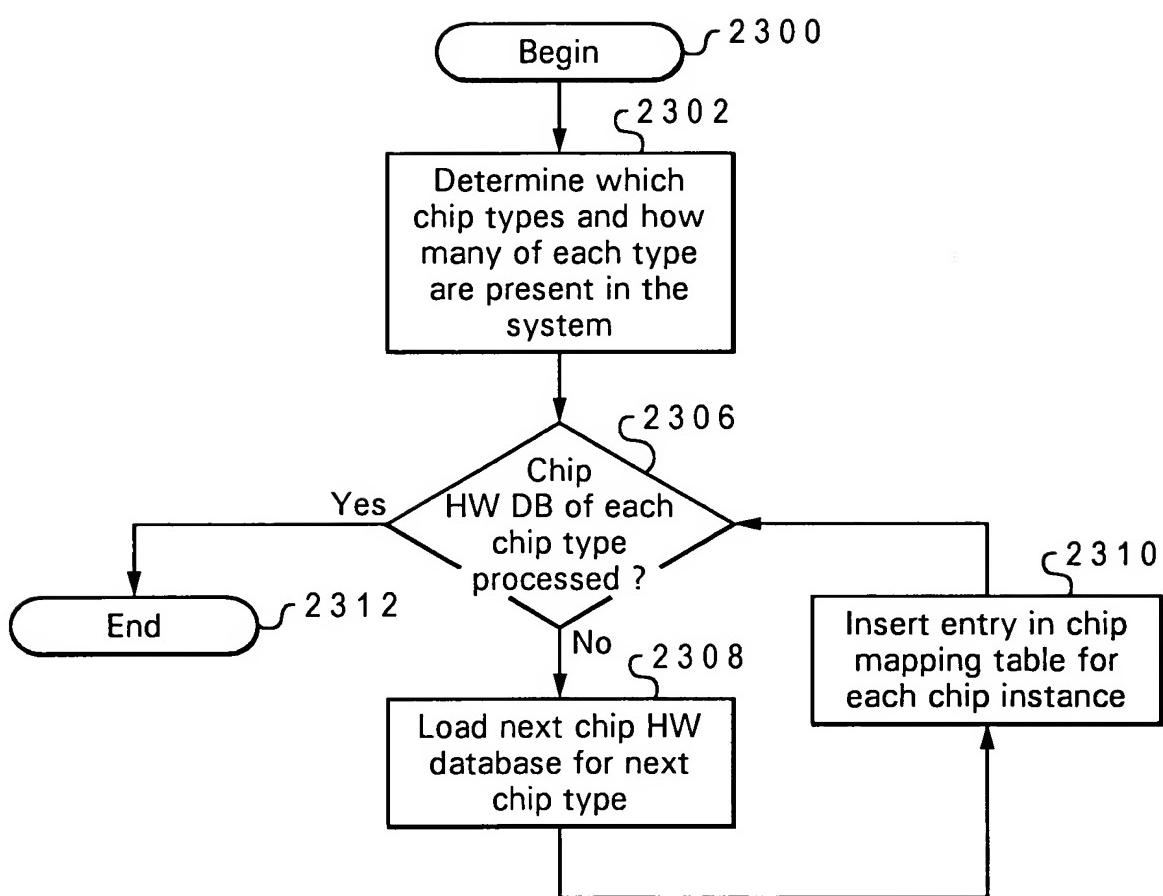


Fig. 23A

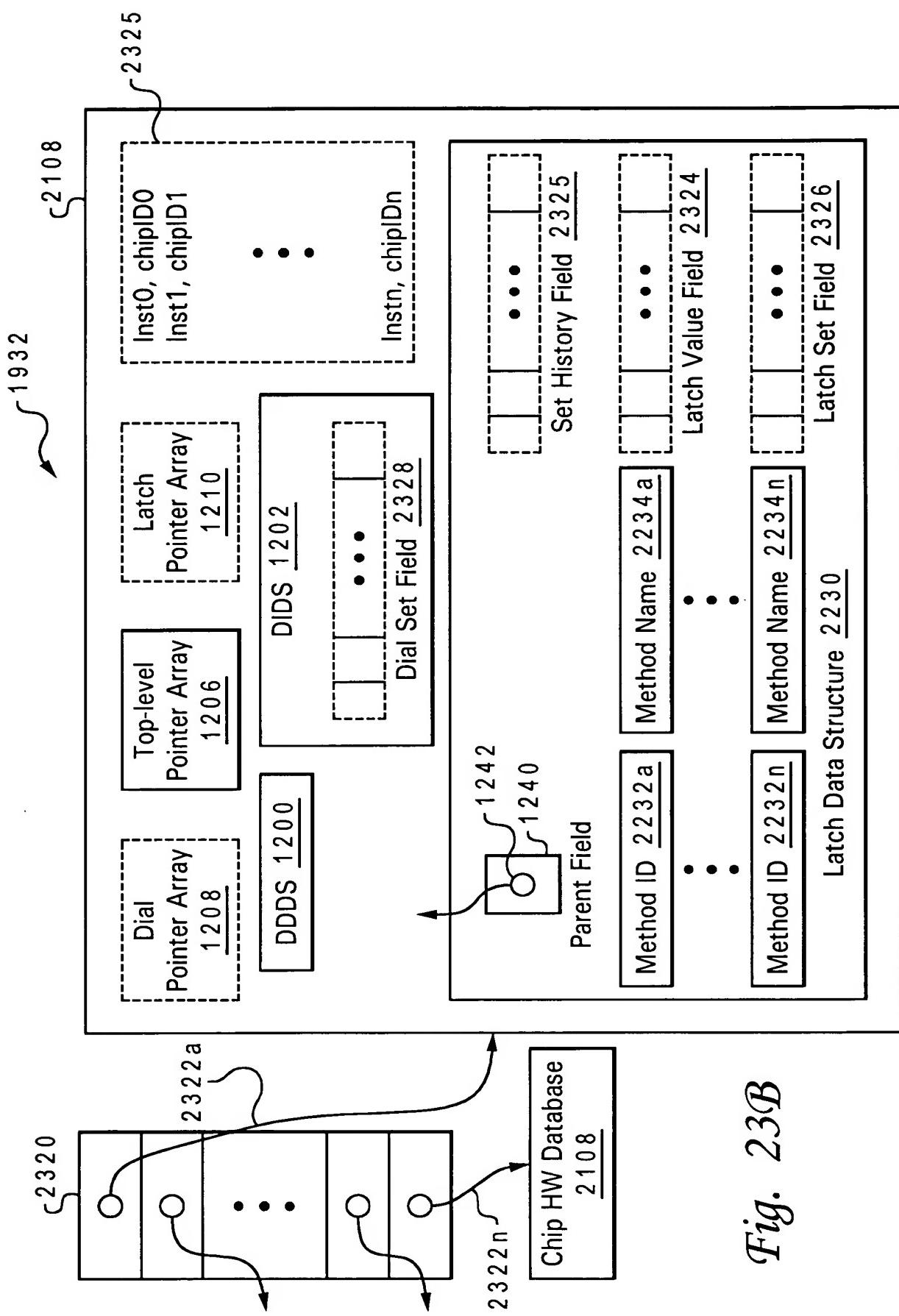


Fig. 23B

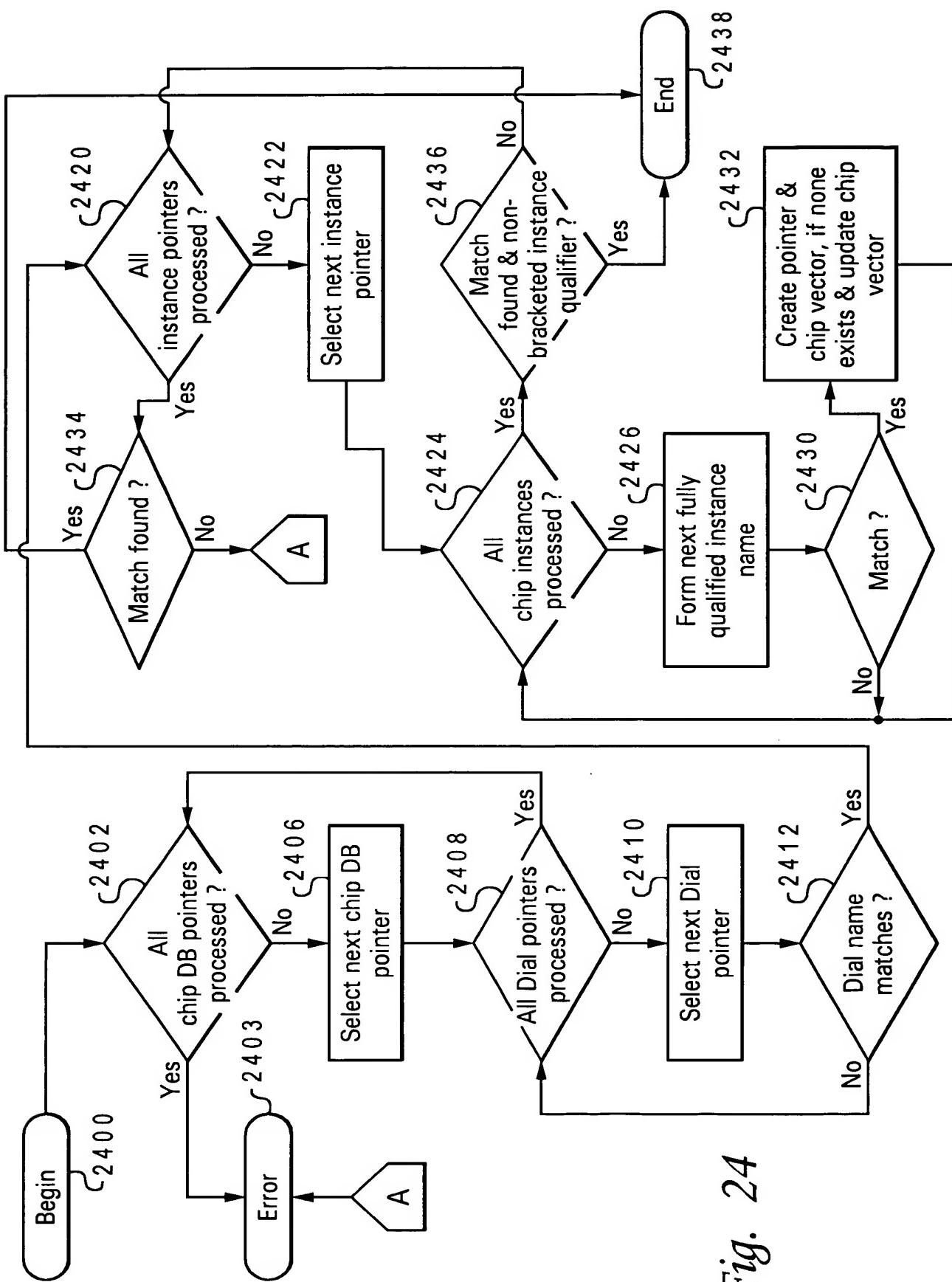


Fig. 24

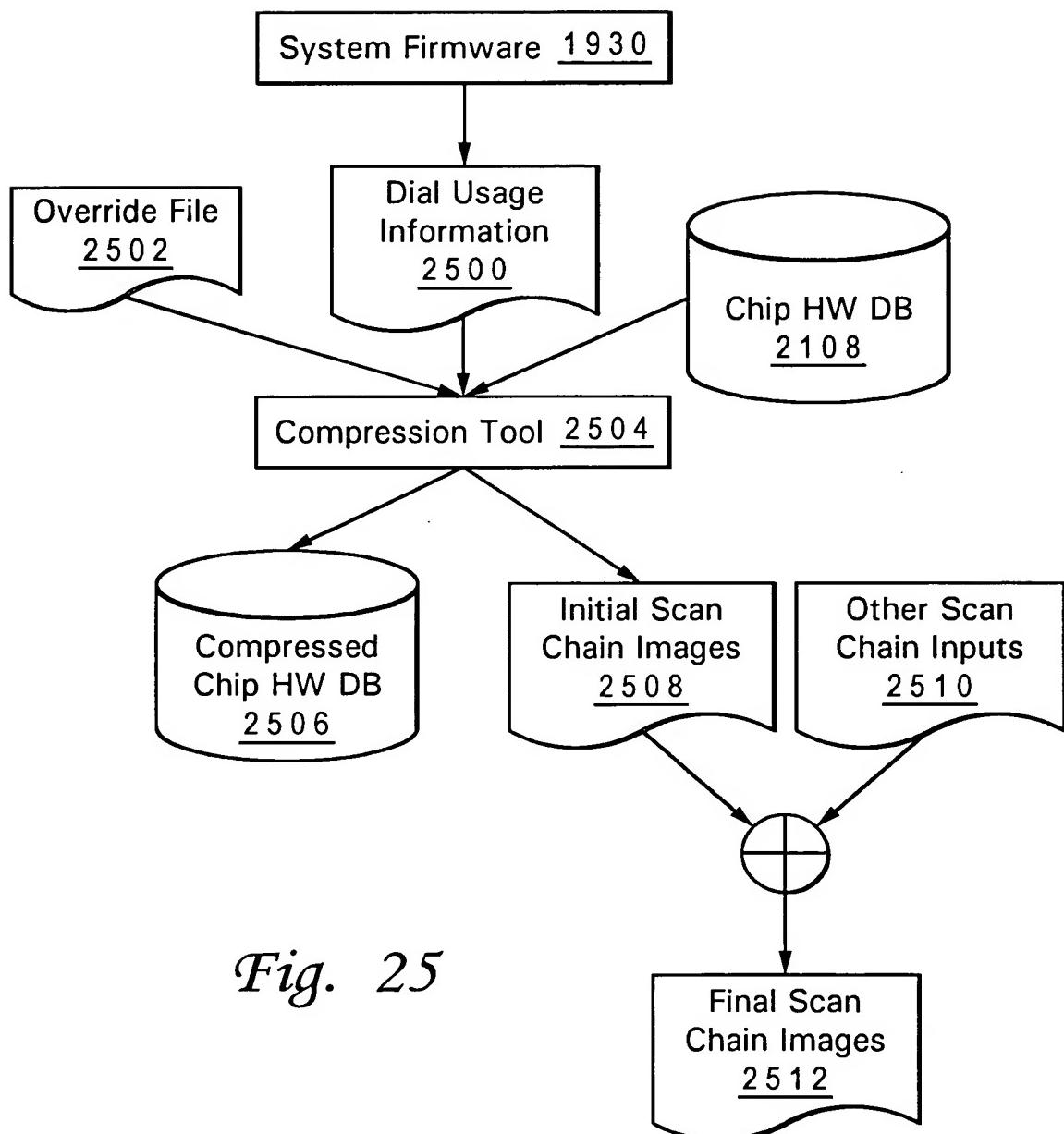


Fig. 25

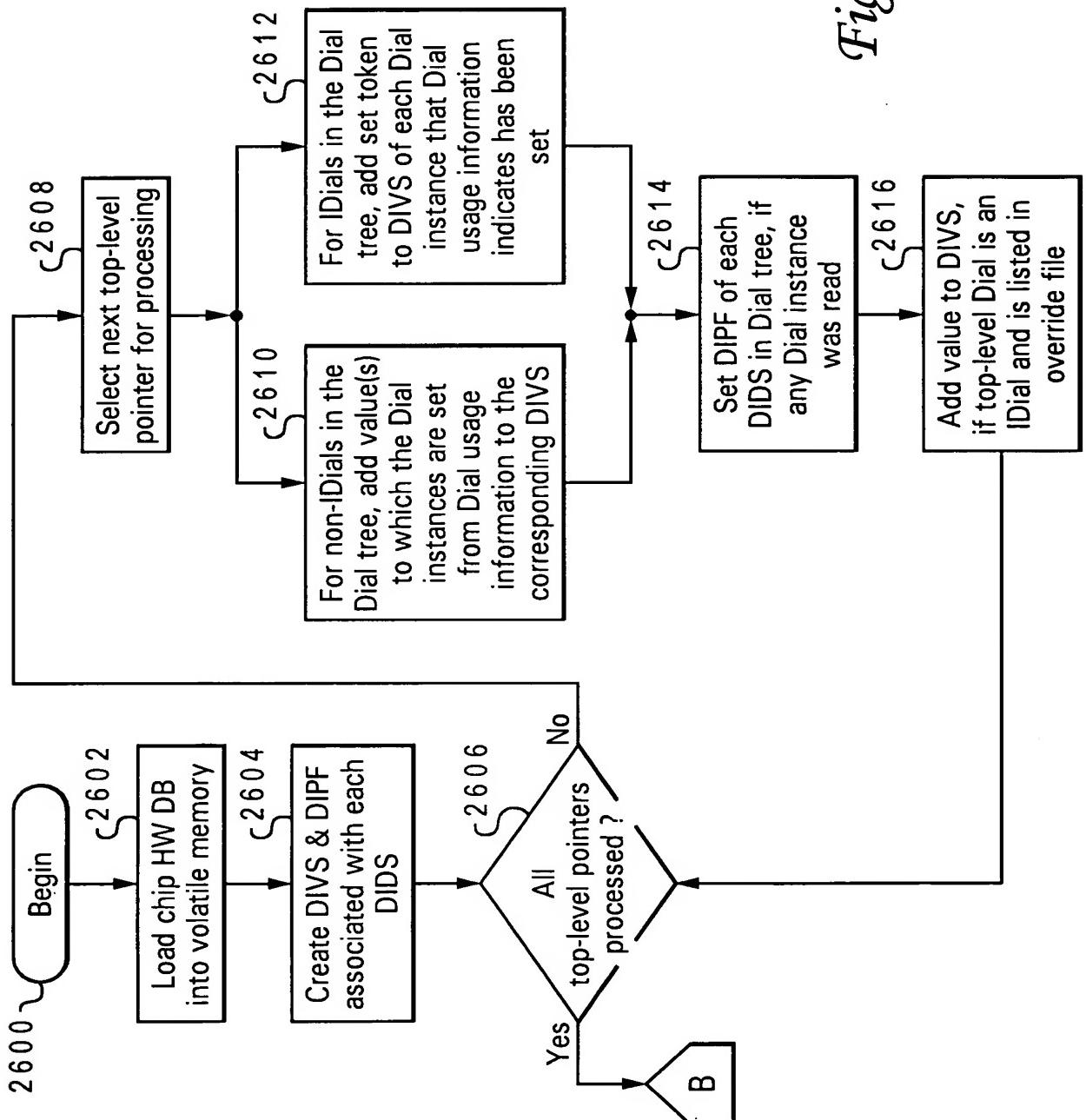


Fig. 26A

Fig. 26B

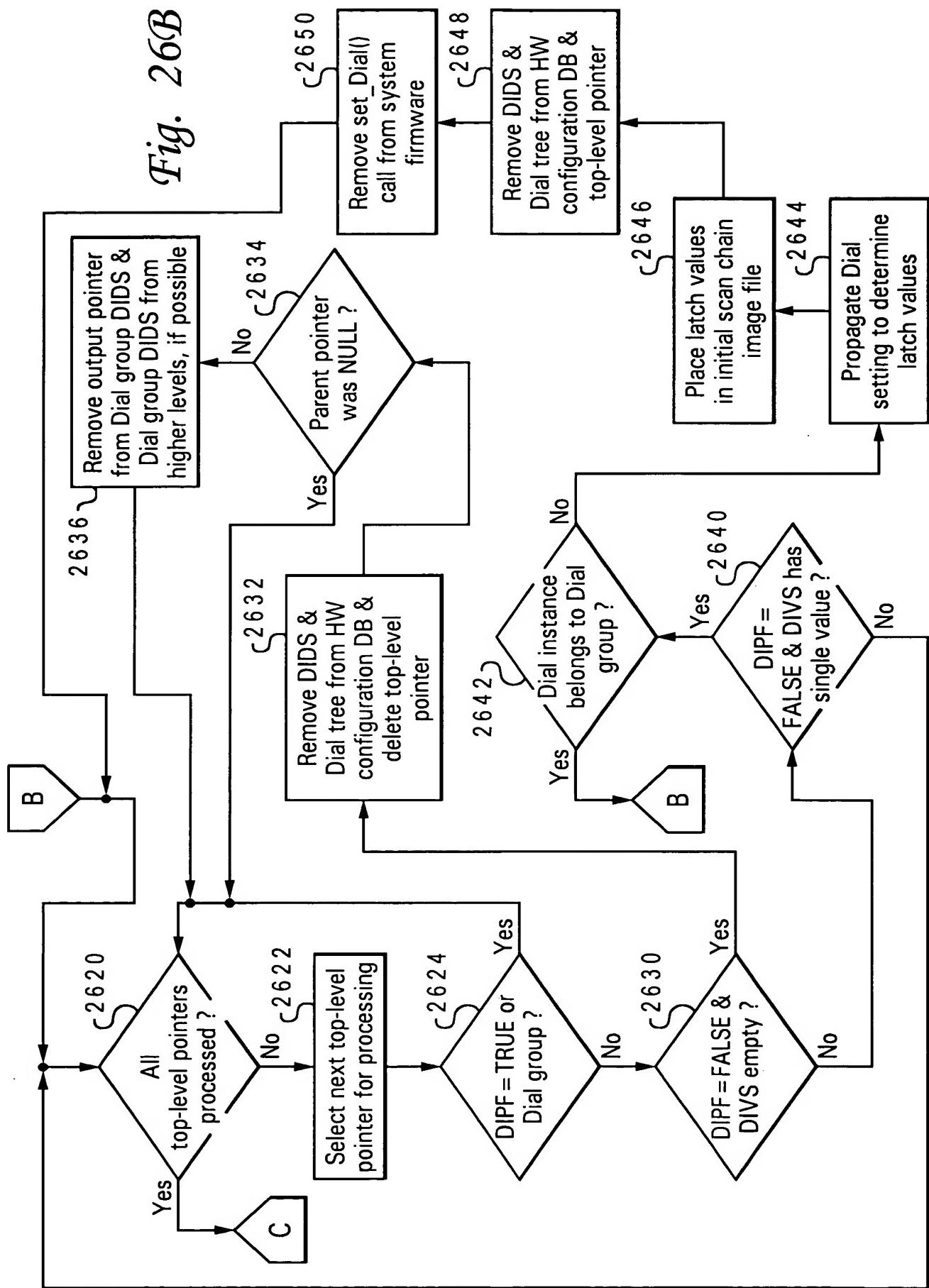
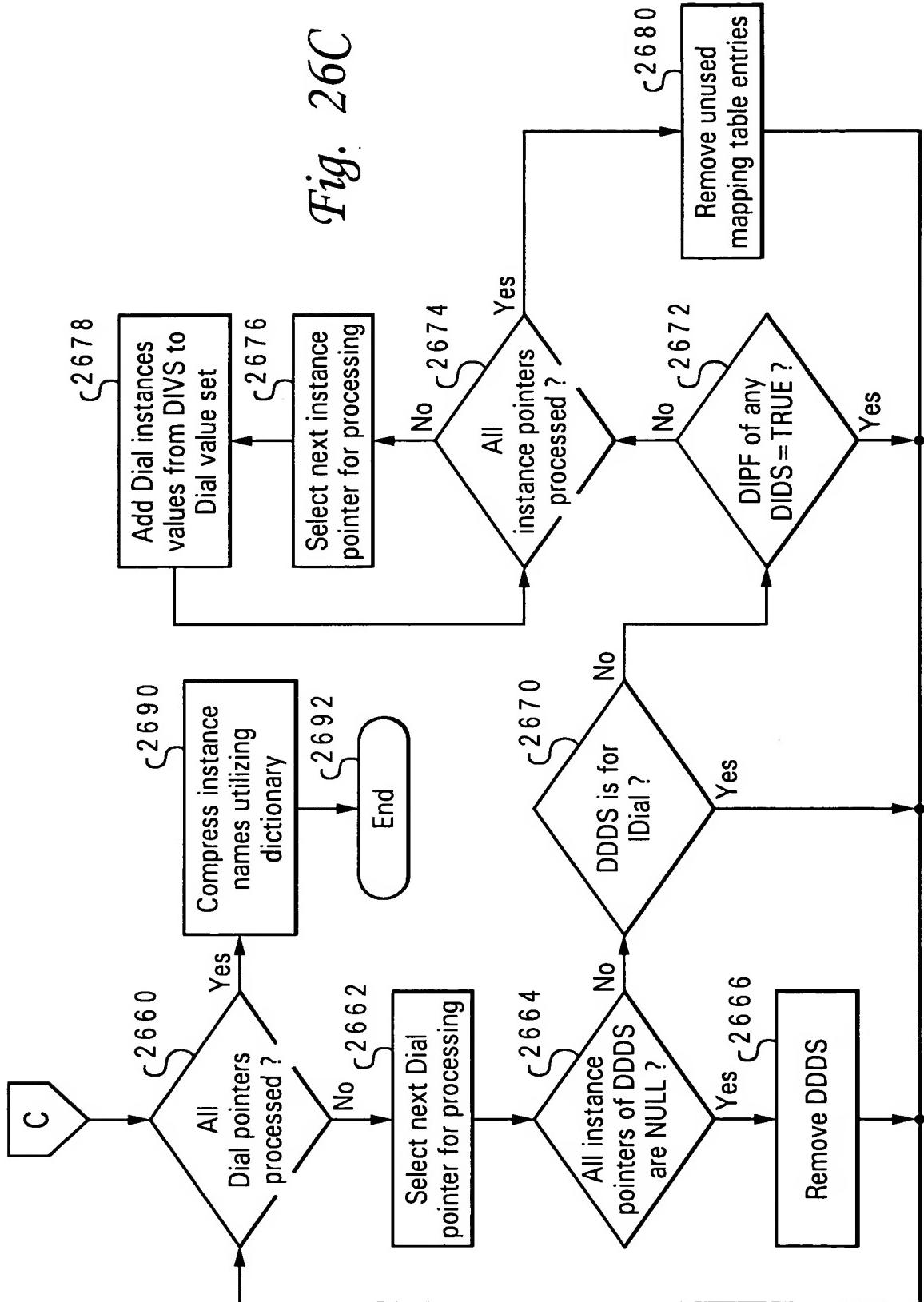


Fig. 26C



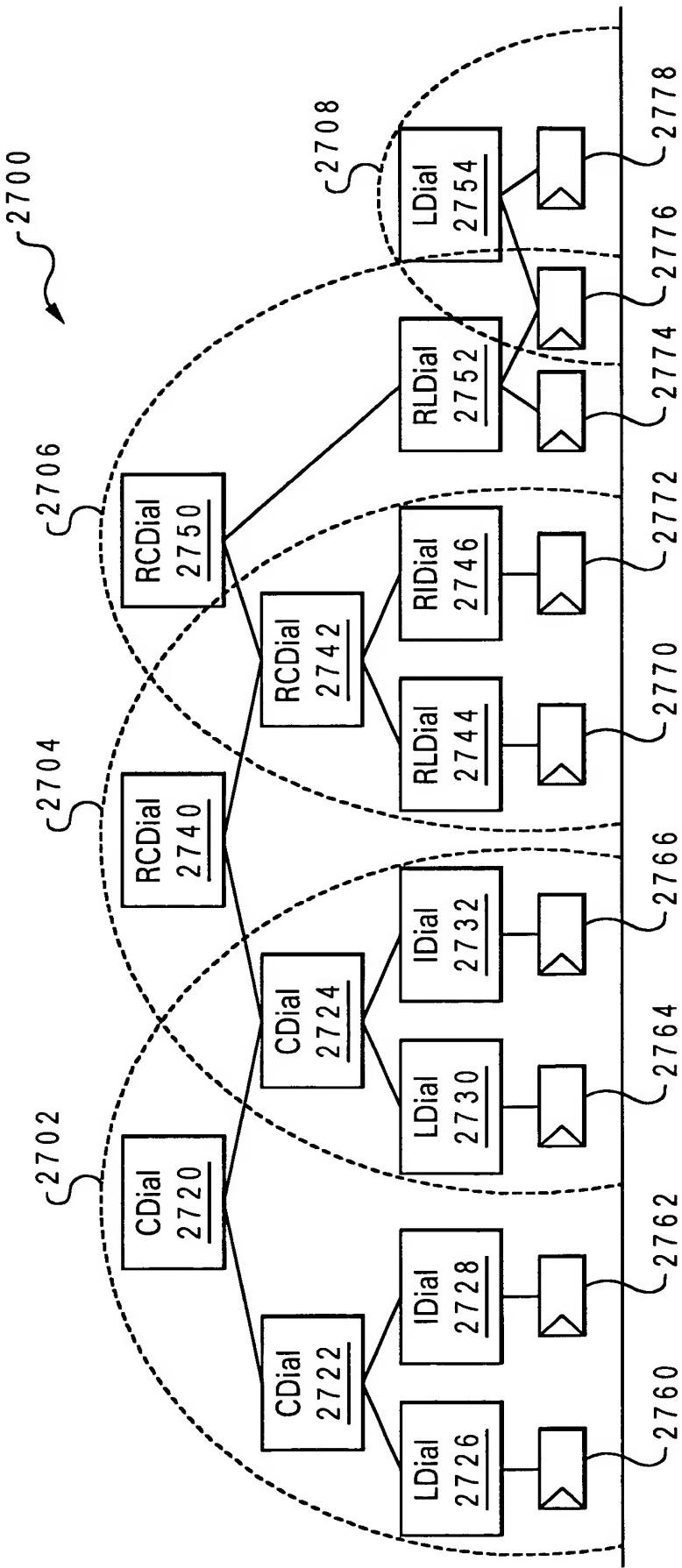


Fig. 27

Fig. 28A

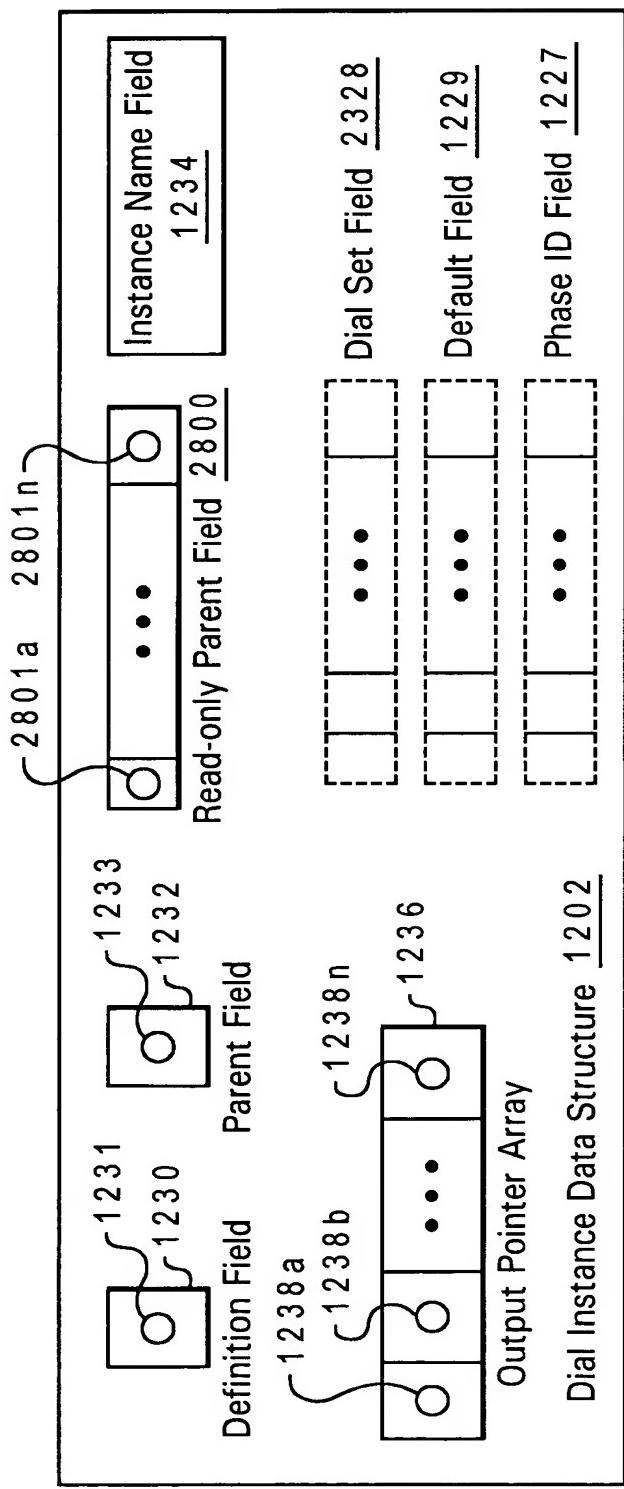
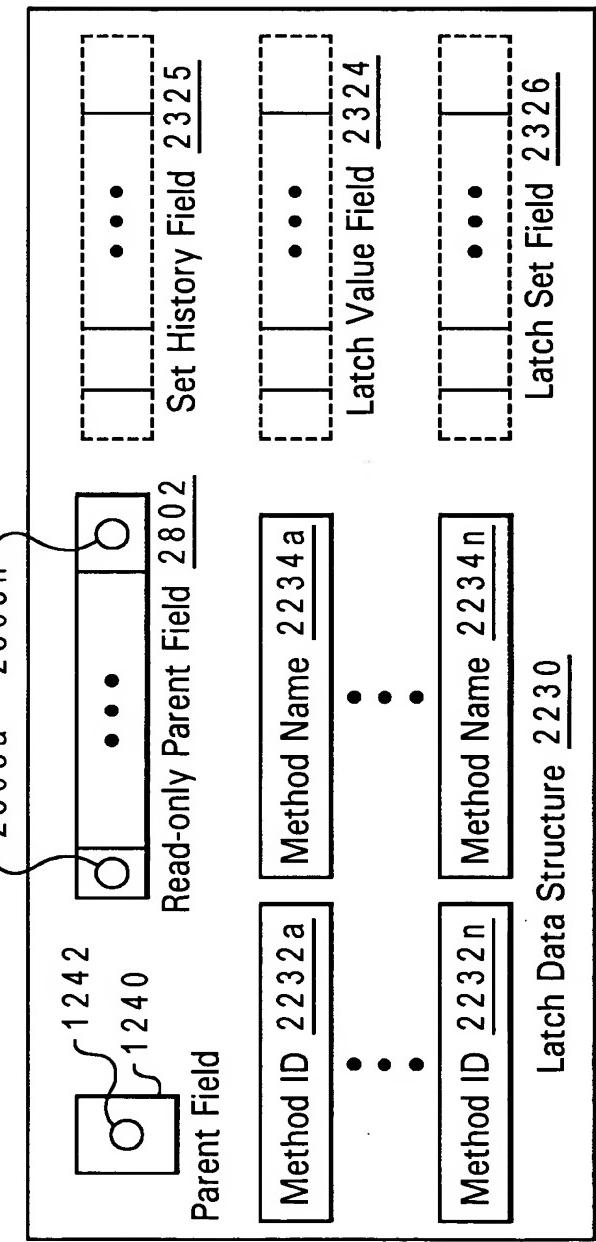
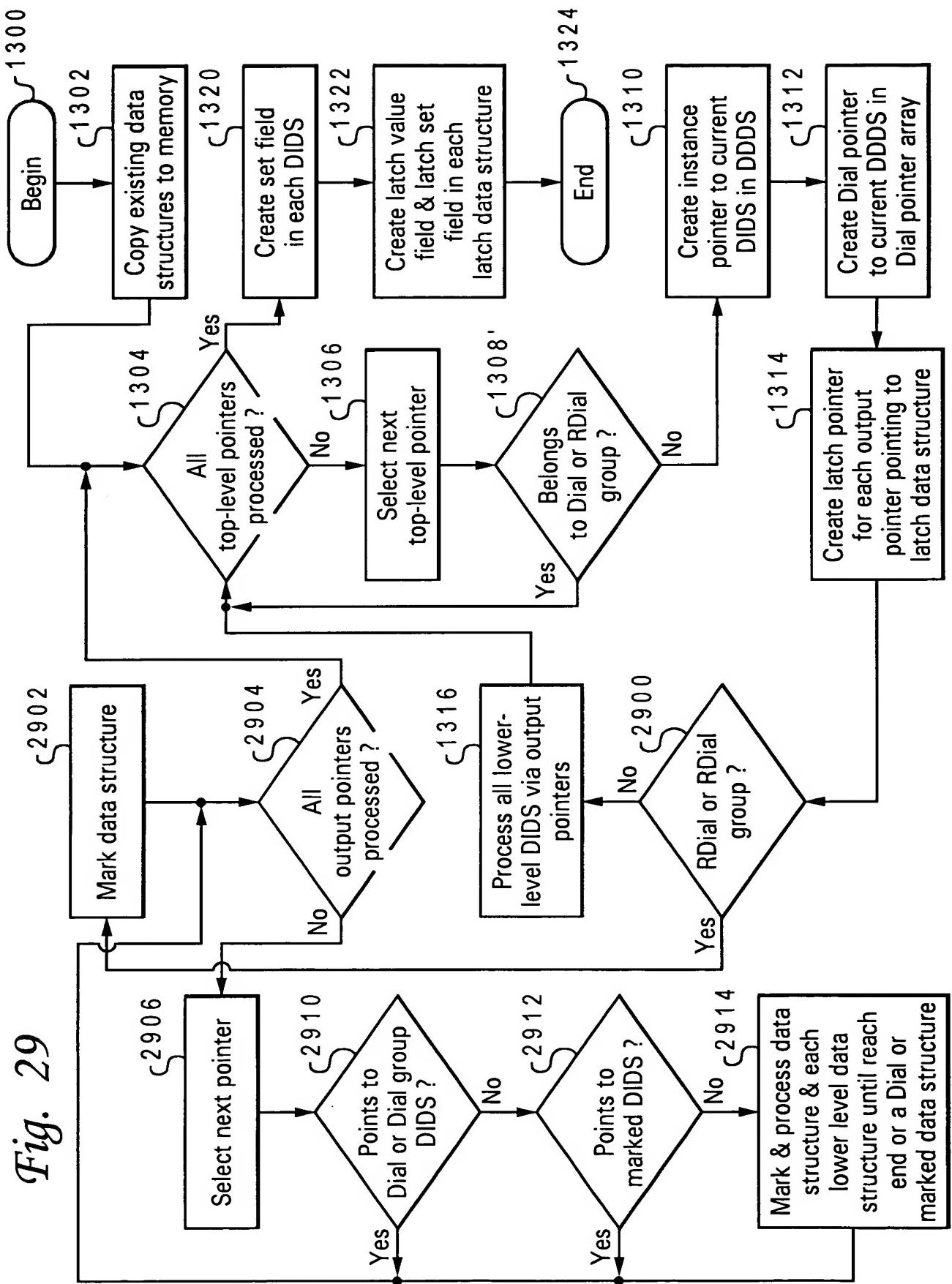
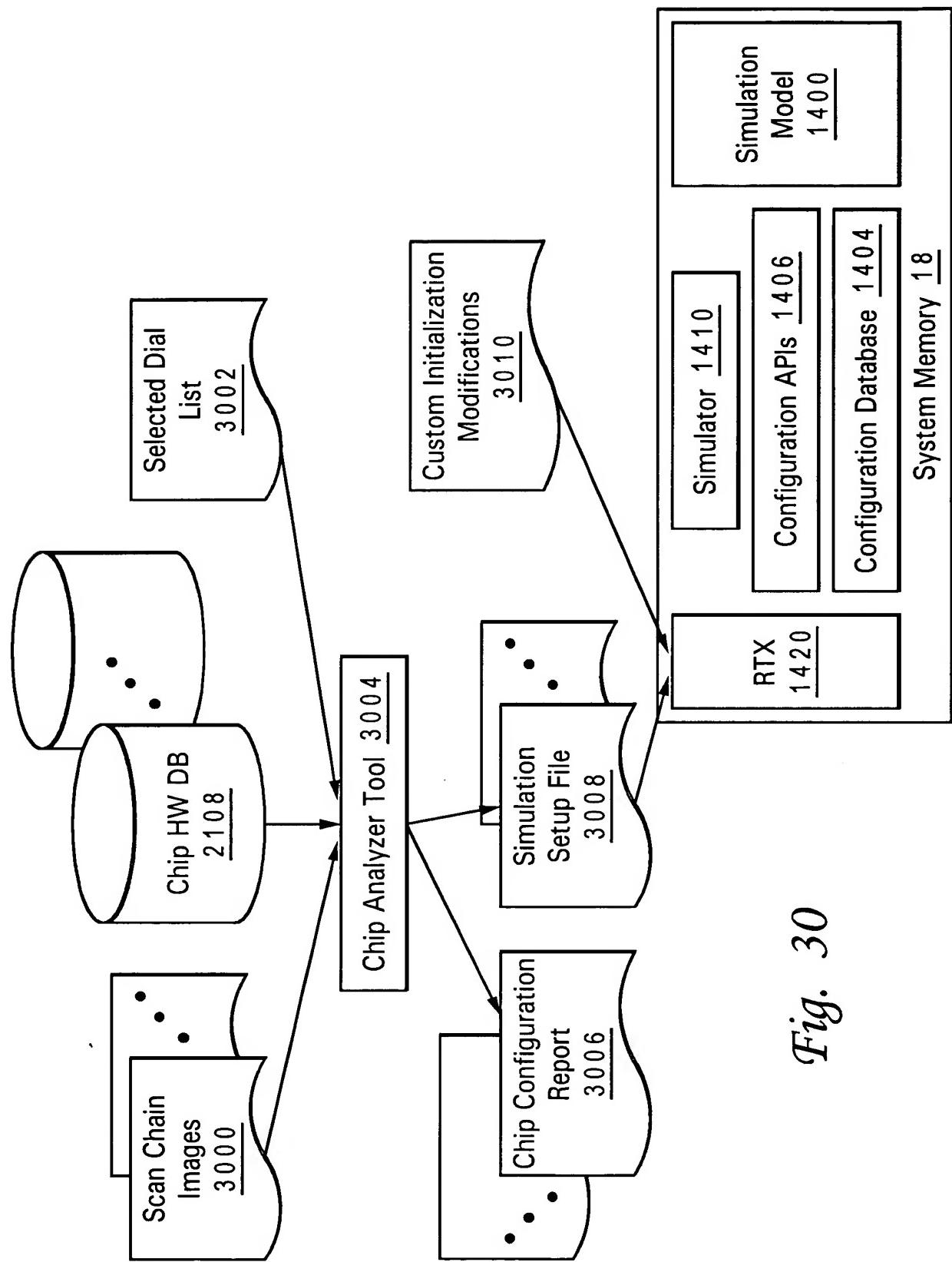


Fig. 28B







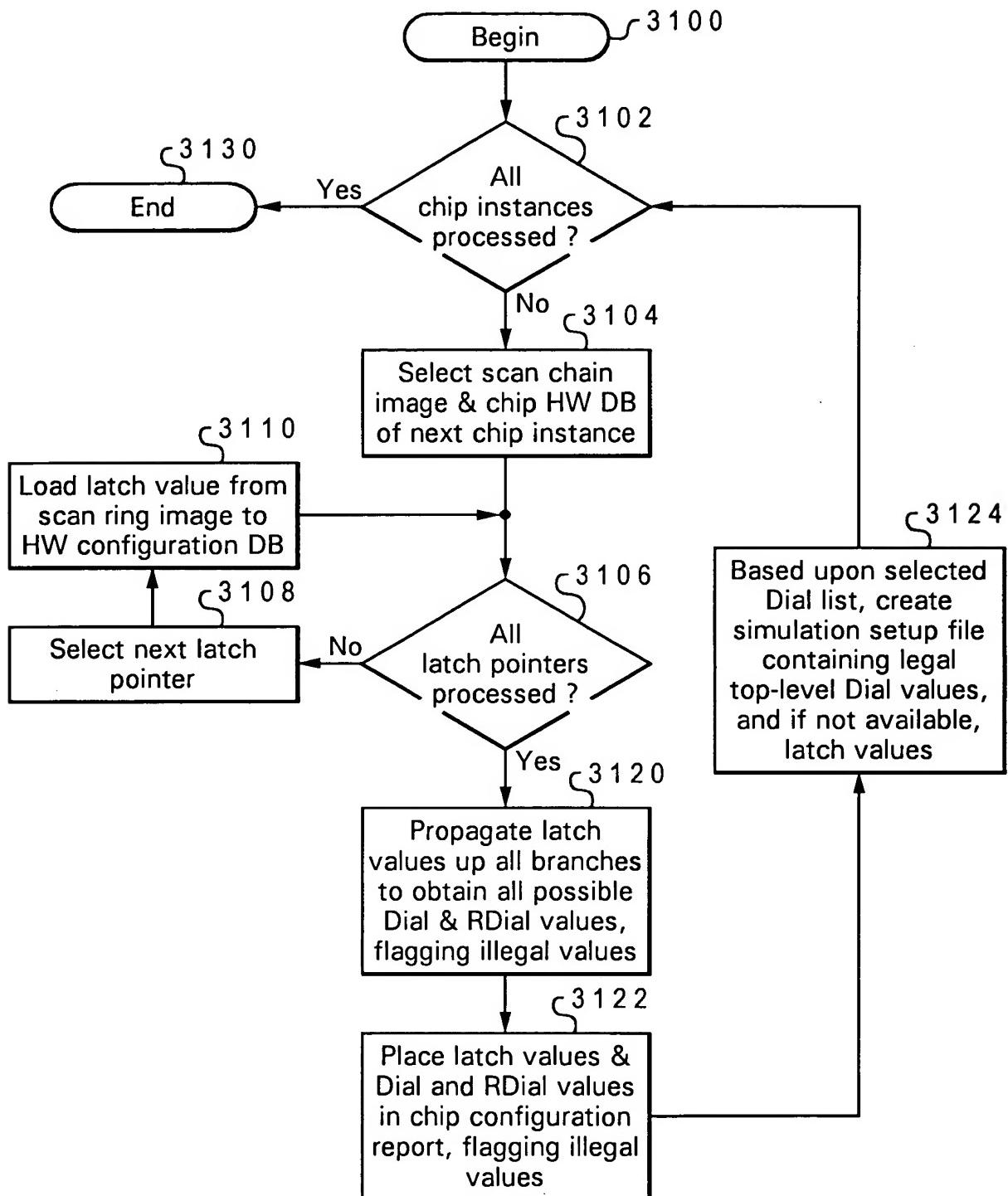


Fig. 31